REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Figure 1; changed case outline M to be available in either a single or dual cavity package. Added vendor CAGE code 0EU86 for device types 05 through 10. -sld	99-04-22	K. A. Cottongim
G	Added device types 11 through 16.	99-08-18	Raymond Monnin
H	Add note to paragraph 1.2.2 and table I, conditions. Add thermal resistance, junction-to-case (θ_{JC}) for all case outlines. Add case outline 9.	00-04-06	Raymond Monnin
J	Table I, I_{CC} change maximum limits and I_{SB} change maximum limits. Figure 1, case outline M, correct diagram adding "c" dimension, lead thickness and change dimension A2 maximum from 0.020" to 0.025".	00-06-19	Raymond Monnin
K	Figure 1, case outline 9, minimum dimension for D2/E2, change 0.990 inches to 0.980 inches and 25.15 mm to 24.89 mm.	01-5-16	Raymond Monnin
L	Table I; Operating supply current (I_{CC}) changed the maximum limit for device types 9 and 15 at f = 50 MHz from 700 mA to 725 mA and for device types 10 and 16 at f = 58.8 MHz from 700 mA to 750 mA. -sld	01-12-21	Raymond Monnin
M	Added device types 17 through 20. -sld	02-11-18	Raymond Monnin
N	Added case outline A. -sld	03-02-24	Raymond Monnin
P	Added case outline B. Added note to paragraph 1.2.4. -sld	03-12-19	Raymond Monnin

REV																				
SHEET																				
REV	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

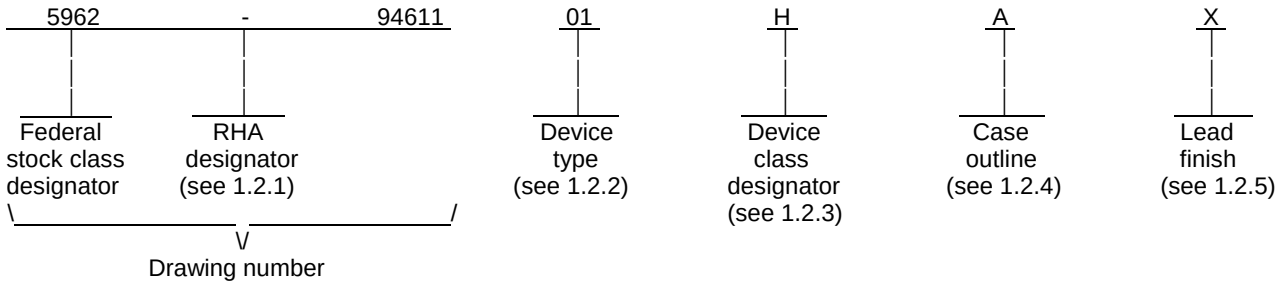
REV STATUS	REV	P	P	P	P	P	P	P	P	P	P	P	P	P
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Gary Zahn	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Michael C. Jones	
	APPROVED BY Kendall A. Cottongim	**MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, 512K x 32-BIT, STATIC RANDOM ACCESS MEMORY, CMOS**
	DRAWING APPROVAL DATE 95-11-13	
	REVISION LEVEL **P**	SIZE A CAGE CODE **67268** **5962-94611** SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type 1/ 2/	Generic number	Circuit function	Access time
01	S512K32-120	512K X 32-BIT SRAM	120 ns
02	S512K32-100	512K X 32-BIT SRAM	100 ns
03	S512K32-85	512K X 32-BIT SRAM	85 ns
04	S512K32-70	512K X 32-BIT SRAM	70 ns
05	S512K32-55	512K X 32-BIT SRAM	55 ns
06	S512K32-45	512K X 32-BIT SRAM	45 ns
07	S512K32-35	512K X 32-BIT SRAM	35 ns
08	S512K32-25	512K X 32-BIT SRAM	25 ns
09	S512K32-20	512K X 32-BIT SRAM	20 ns
10	S512K32-17	512K X 32-BIT SRAM	17 ns
11	S512K32-55	512K X 32-BIT SRAM	55 ns
12	S512K32-45	512K X 32-BIT SRAM	45 ns
13	S512K32-35	512K X 32-BIT SRAM	35 ns
14	S512K32-25	512K X 32-BIT SRAM	25 ns
15	S512K32-20	512K X 32-BIT SRAM	20 ns
16	S512K32-17	512K X 32-BIT SRAM	17 ns
17	S512K32-15	512K X 32-BIT SRAM	15 ns
18	S512K32-12	512K X 32-BIT SRAM	12 ns
19	S512K32-15	512K X 32-BIT SRAM	15 ns
20	S512K32-12	512K X 32-BIT SRAM	12 ns

1/ Due to the nature of the 4 transistor design of the die used in these device types, topologically pure testing is important, particularly for high reliability applications. The device manufacturer should be consulted concerning their testing methods and algorithms

2/ Device types 11 through 18 are not tested to data retention supply voltage (V_{DR}) and data retention current (I_{CCDR1}). See table I.

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A	See figure 1	68	Co-fired ceramic, quad flatpack, single cavity
B	See figure 1	68	Ceramic, quad flatpack, single cavity
M 3/	See figure 1	68	Co-fired ceramic, single/dual cavity, quad flatpack
T	See figure 1	66	Hex-in-line, single cavity, with standoffs
U	See figure 1	66	Hex-in-line, single cavity, with standoffs
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y	See figure 1	68	Ceramic, quad flatpack, single cavity
9 3/	See figure 1	68	Ceramic, quad flatpack, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

3/ Due to the short leads of case outlines M (single cavity) and case outline 9, caution should be taken if the system application is to be used where extreme thermal transitions can occur. Case outline A can be used if longer leads are necessary.

1.3 Absolute maximum ratings. 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_g)	-0.5 V dc to V_{CC} +0.5 V dc
Power dissipation (P_D):	
Device types 01-04 and 17-20	2.2 W
Device types 05, 06, 11, and 12	3.2 W
Device types 07, 08, 13, and 14	3.6 W
Device types 09, 10, 15, and 16	4.4 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline A and M	9.27°C/W
Case outlines T, U, and X	4.160°C/W
Case outline Y	5.251°C/W
Case outlines B and 9	1.495°C/W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc +4.5 V dc ≤ V_{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC parameters							
Operating supply current	I_{CC}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc 3/ f = 5 MHz f = 5 MHz f = 18.2 MHz f = 22.2 MHz f = 28.6 MHz f = 40 MHz f = 50 MHz f = 58.8 MHz f = 66.67 MHz f = 83.3 MHz	1,2,3	01-04 05-16 05,11 06,12 07,13 08,14 09,15 10,16 17,19 18,20		200 600 625 635 650 675 725 750 200 250	mA
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc 3/ f = 5 MHz f = 5 MHz f = 18.2 MHz f = 22.2 MHz f = 28.6 MHz f = 40 MHz f = 50 MHz f = 58.8 MHz f = 66.67 MHz f = 83.3 MHz	1,2,3	01-04 05-16 05,11 06,12 07,13 08,14 09,15 10,16 17-20 17-20		4 80 150 150 190 240 280 320 80 80	mA
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = +4.5 V dc, I_{OL} = 2.1 mA	1,2,3	01-06, 11,12		0.4	V
		V_{CC} = +4.5 V dc, I_{OL} = 8 mA		07-10, 13-20		0.4	
Output high voltage	V_{OH}	V_{CC} = +4.5 V dc, I_{OL} = -1.0 mA	1,2,3	01-06, 11,12	2.4		V
		V_{CC} = +4.5 V dc, I_{OL} = -4.0 mA		07-10, 13-20	2.4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc +4.5 V dc ≤ V_{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data retention characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC}$ - 0.2 V dc	1,2,3	01-10	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3 V dc	1,2,3	01-04		1.6	mA
				05-10		28	
				19,20		32	
Capacitance							
$\overline{OE}$ capacitance 4/	C_{OE}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
$\overline{WE}$ 1-4 capacitance 4/	C_{WE}	V_{OUT} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
$\overline{CS}$ capacitance 4/	C_{CS}	V_{IN} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
D_{0-31} capacitance 4/	$C_{I/O}$	V_{OUT} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		20	pF
A_{0-16} capacitance 4/	C_{AD}	V_{OUT} = 0 V dc, f = 1.0 MHz, T_A = +25°C	4	All		50	pF
Functional tests							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle timing characteristics							
Read cycle timing	t_{RC}	See figure 4.	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05,11	55		
				06,12	45		
				07,13	35		
				08,14	25		
				09,15	20		
				10,16	17		
				17,19	15		
				18,20	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc +4.5 V dc ≤ V_{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle timing characteristics - Continued.							
Address access timing	t_{AA}	See figure 4.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16 17,19 18,20		120 100 85 70 55 45 35 25 20 17 15 12	ns
Output hold from address change	t_{OH}	See figure 4.	9,10,11	01-04 05-10 11-20	5 0 0		ns
Chip select access timing	t_{ACS}	See figure 4.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16 17,19 18,20		120 100 85 70 55 45 35 25 20 17 15 12	ns
Output enable to output valid	t_{OE}	See figure 4.	9,10,11	01 02 03 04 05-07 11-13 08,14 09,15 10,16 17,19 18,20		60 50 40 35 25 25 12 10 9 8 7	ns
Chip select to output in low impedence 4/	t_{CLZ}	See figure 4.	9,10,11	01,02 03,04 05-07 11-13 08-10 14-20	10 10 4 4 2 2		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle timing characteristics - Continued.							
Output enable to output in low impedence 4/	t_{OLZ}	See figure 4.	9,10,11	01-04 05-20	5 0		ns
Chip select high to output in high impedence 4/	t_{CHZ}	See figure 4.	9,10,11	01,02 03,04 05,06 11,12 07,13 08-10 14-16 17,19 18,20		35 25 20 20 15 12 12 8 7	ns
Chip enable high to output in high impedence 4/	t_{OHZ}	See figure 4.	9,10,11	01,02 03,04 05,06 11,12 07,13 08-10 14-16 17,19 18,20		35 25 20 20 15 12 12 8 7	ns
Write cycle AC timing characteristics.							
Write cycle time	t_{WC}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16 17,19 18,20	120 100 85 70 55 45 35 25 20 17 15 12		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle AC timing characteristics - Continued.							
Chip select to end of write	t_{CW}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,10 15,16 17,19 18,20	120 80 75 60 50 35 30 20 15 15 12 10		ns
Address valid to end of write	t_{AW}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,10 15,16 17,19 18,20	100 80 75 60 50 35 30 20 15 15 12 10		ns
Data valid to end of write	t_{DW}	See figure 5.	9,10,11	01,02 03,04 05,06 11,12 07,13 08,14 09,10 15,16 17,19 18,20	40 30 25 25 20 15 12 12 10 8		ns
Address setup time	t_{AS}	See figure 5.	9,10,11	01-04 05-10 11-20	0 2 2		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle AC timing characteristics - Continued.							
Write pulse width	t_{WP}	See figure 5.	9,10,11	01,02 03,04 05,11 06,12 07,13 08,14 09,10 15,16 17,19 18,20	60 50 40 35 25 17 15 15 12 10		ns
Write enable to output in high impedence 4/	t_{WHZ}	See figure 5.	9,10,11	01,02 03,04 05,06 11,12 07,13 08,14 09,15 10,16 17,19 18,20		35 25 20 20 15 13 11 9 8 7	ns
Address hold time	t_{AH}	See figure 5.	9,10,11	01-06 11,12 07,08 13,14 09,15 17-20 10,16	5 5 2 2 1 1 0		ns
Output active from end of write 4/	t_{OW}	See figure 5.	9,10,11	01-04 05-20	5 0		ns
Data hold time	t_{DH}	See figure 5.	9,10,11	All	0		ns

1/ Due to the nature of the 4 transistor design of the die used in these device types, topologically pure testing is important, particularly for high reliability applications. The device manufacturer should be consulted concerning their testing methods and algorithms

2/ Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V
Input rise and fall times: 5 nanoseconds for device types 01-16 and 3 nanoseconds for device types 17-20.
Input and output timing reference level: 1.5 V ± 0.5 V
Output loading: see Figure 7.
Unless otherwise specified, the DC test conditions are as follows:
V_{IL} = 0.3 V and V_{IH} = V_{CC} - 0.3 V

3/ f = 1 / t_{AA}.

4/ Parameters shall be tested as part of device characterization and after design and process change. Parameters shall be to the limits specified in table 1 for all lots not specifically tested.

Case outline A.

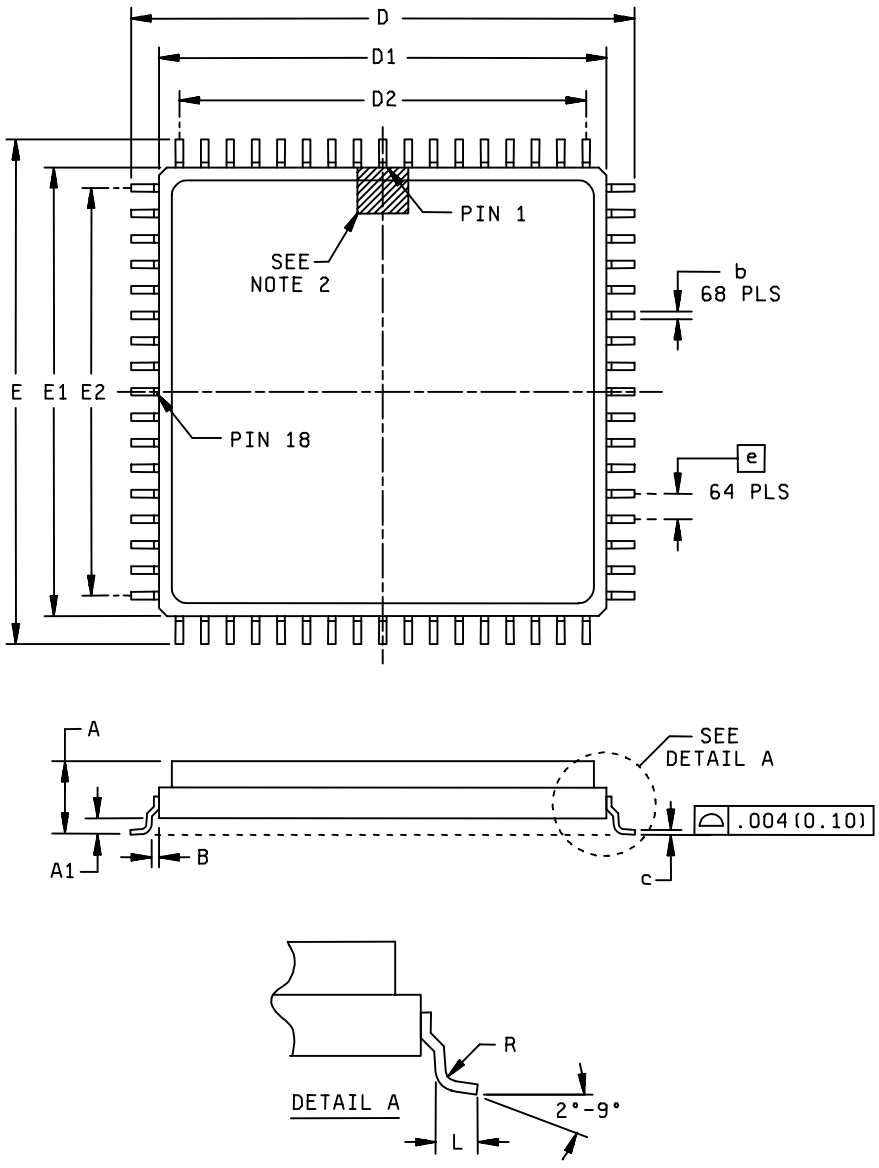


FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-94611
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL P	SHEET 13

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		5.10		.200
A1	1.37		.054	
b	0.33	0.43	.013	.017
B	0.25 TYP		.010 TYP	
c	0.23	0.30	.009	.012
D/E	24.9	25.4	.980	1.000
D1/E1	22.10	22.61	.870	.890
D2/E2	20.32 BSC		.800 BSC	
e	1.27 BSC		.050 BSC	
L	0.89	1.14	.035	.045
R	0.25 TYP		.010 TYP	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Details of pin 1 identifier are optional, but must be located within the zone indicated.

FIGURE 1. Case outlines - Continued.

Case outline M.

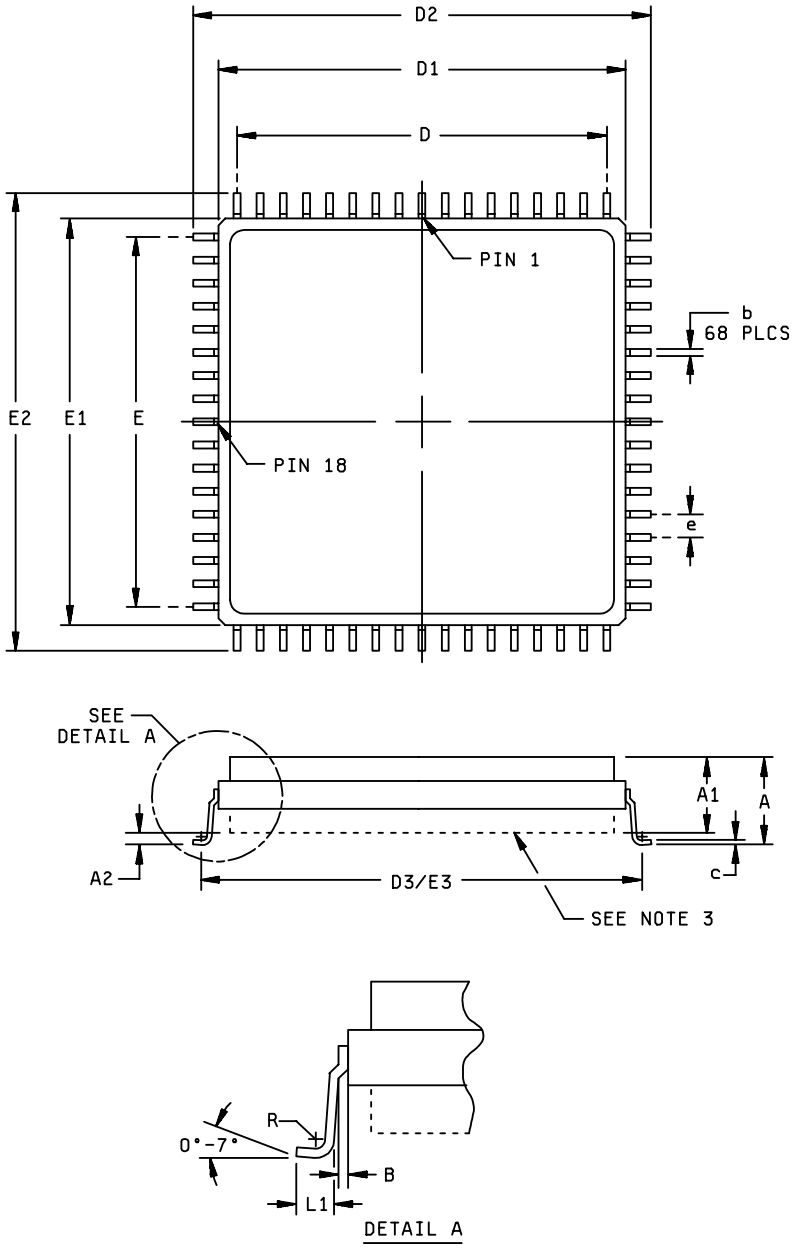


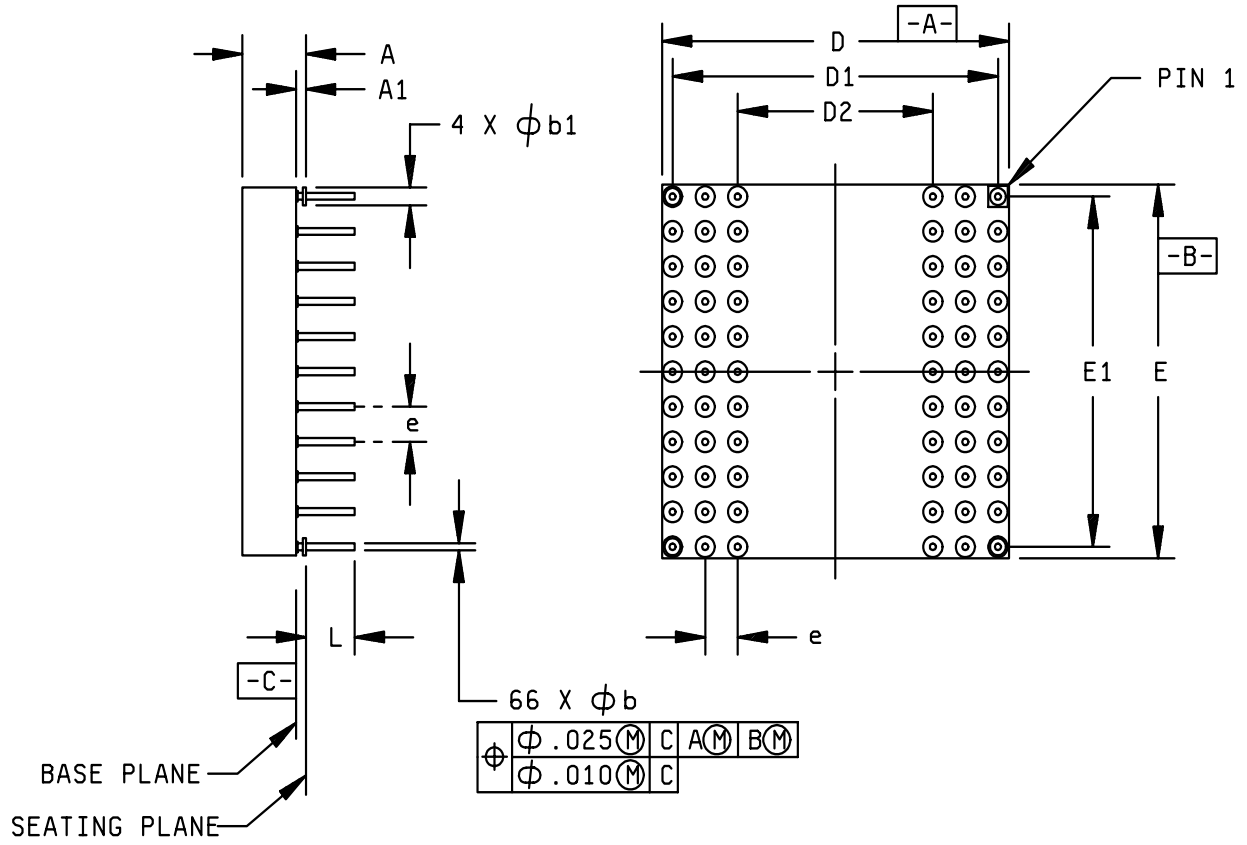
FIGURE 1. Case outline(s).

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.12	5.08	.123	.200
A1	2.30	4.72	.118	.186
A2	0.00	0.64	.000	.025
b	0.33	0.43	.013	.017
B	0.25 REF		.010 REF	
c	0.15	0.30	.006	.012
D/E	20.32 BSC		.800 BSC	
D1/E1	22.10	22.61	.870	.890
D2/E2	24.89	25.40	.980	1.000
D3/E3	23.77	24.28	.936	.956
e	1.27 BSC		.050 BSC	
R	0.13		.005	
L1	0.89	1.14	.035	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M may either be a single cavity or a dual cavity package. Dimension A2 is measured between the lowest horizontal plane of the package and the seating plane of the lead(s).

FIGURE 1. Case outline(s) - Continued.

Case outline T.

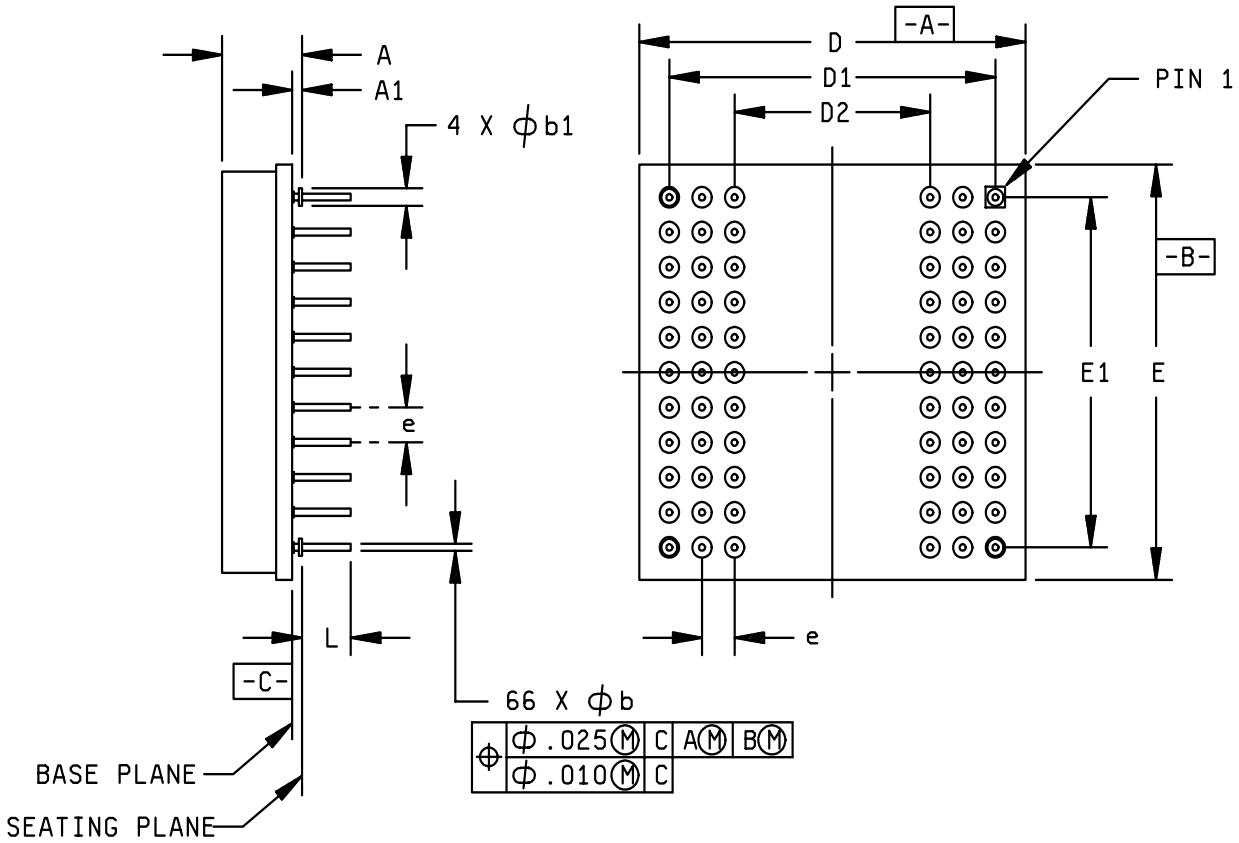


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.65	4.60	.144	.181
A1	0.64	0.89	.025	.035
øb	0.41	0.51	.016	.020
øb1	1.14	1.40	.045	.055
D/E	27.05	27.55	1.065	1.085
D1/E1	25.40 TYP		1.000 TYP	
D2	15.24 TYP		.600 TYP	
e	2.54 TYP		.100 TYP	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline U.

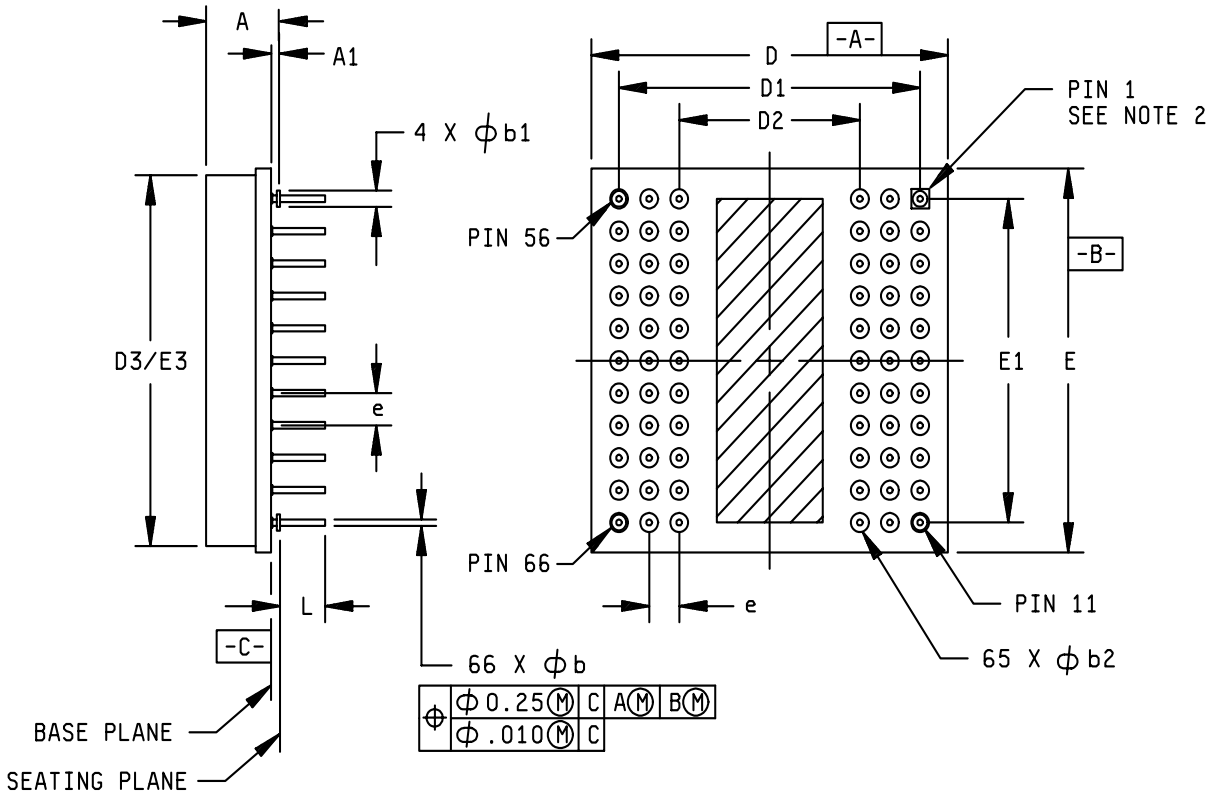


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.08	6.22	.200	.245
A1	0.64	0.89	.025	.035
øb	0.41	0.51	.016	.020
øb1	1.14	1.40	.045	.055
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 TYP		1.000 TYP	
D2	15.24 TYP		.600 TYP	
e	2.54 TYP		.100 TYP	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline X.

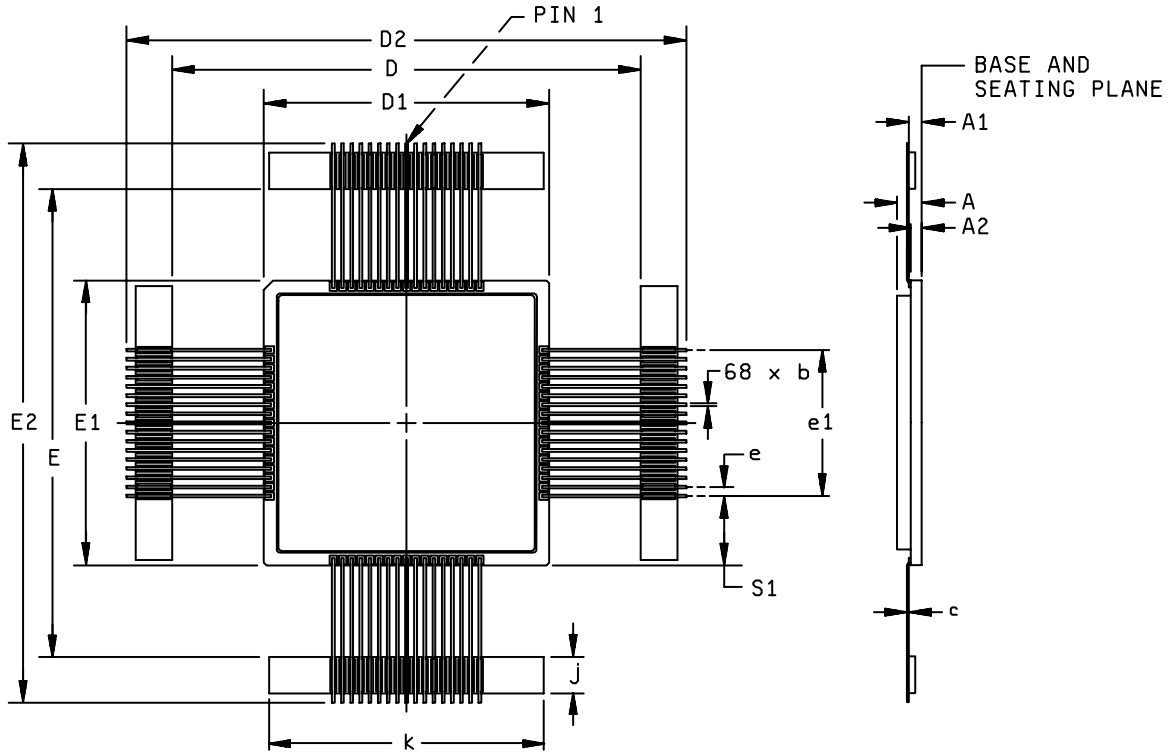


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.83	6.22	.190	.245
A1	0.64	0.89	.025	.035
øb	0.41	0.51	.016	.020
øb1	1.14	1.40	.045	.055
øb2	1.65	1.91	.065	.075
D/E	34.80	35.56	1.370	1.400
D1/E1	25.40 TYP		1.000 TYP	
D2	15.24 TYP		.600 TYP	
D3/E3	34.04	34.29	1.340	1.350
e	2.54 TYP		.100 TYP	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only. Pin 1 is identified by .070 " square pad.
3. For solder lead finish, dimension ϕb will increase by +.003" (+0.008 mm).

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

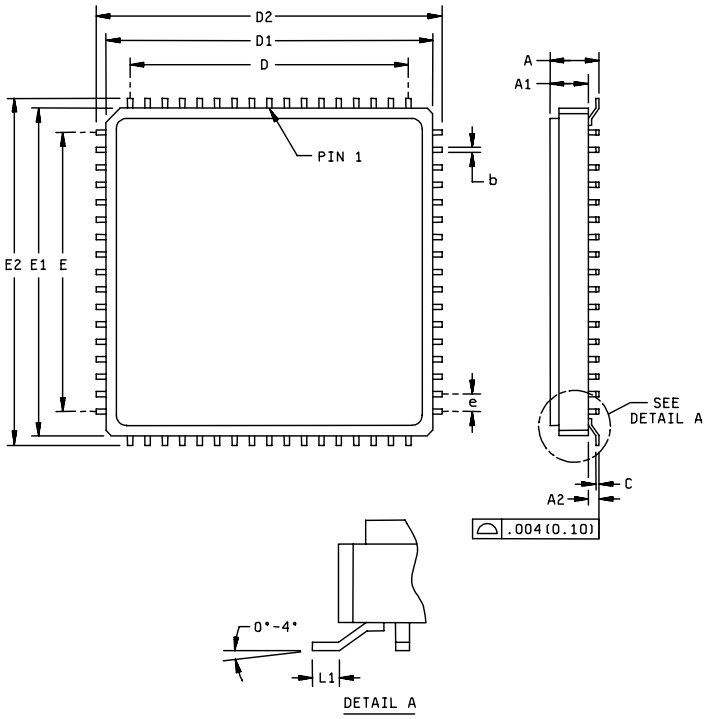


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	3.56	.115	.140
A1	1.14	1.91	.045	.075
A2	1.14	1.39	.045	.055
b	0.31	0.46	.012	.018
c	0.23	0.31	.009	.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	84.20	2.885	3.315
e	1.27 BSC		.050 BSC	
e1	20.32 BSC		.800 BSC	
j	4.83	5.33	.190	.210
k	37.72	38.48	1.485	1.515
S1	9.65 BSC		.380 BSC	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. For solder lead finish, dimension b will increase by +.003" (+0.008 mm).

FIGURE 1. Case outline(s) - Continued.

Case outline B.

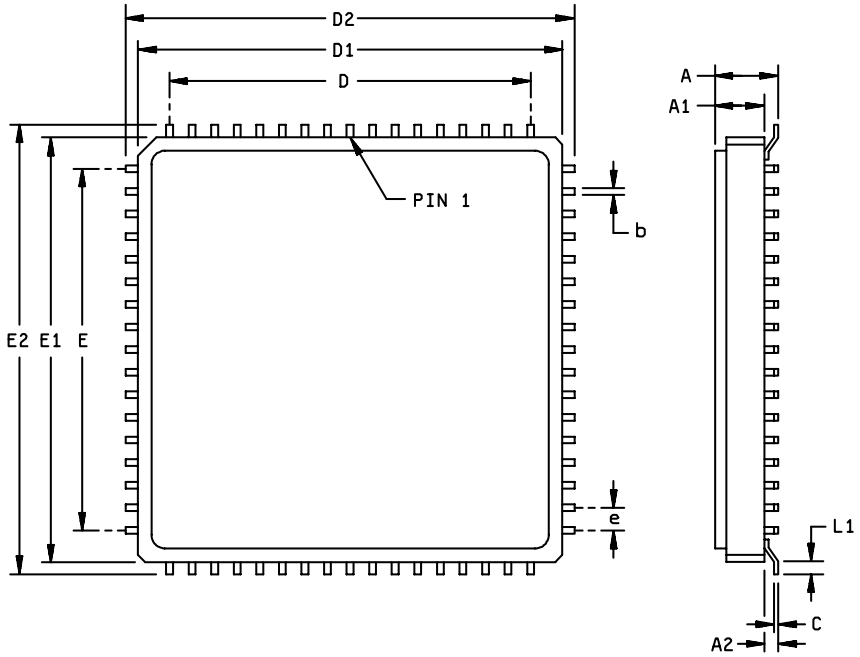


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.06		.160
A1		2.79		.110
A2	1.12	1.42	.044	.056
b	0.33	0.43	.013	.017
C	0.15	0.25	.006	.010
D/E	20.32 BSC		.800 BSC	
D1/E1	23.65	24.10	.931	.949
D2/E2	24.89	25.40	.980	1.000
e	1.27 BSC		.050 BSC	
L1	0.51	1.14	.020	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline 9.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.56		.140
A1		2.79		.110
A2	0.46	0.76	.018	.030
b	0.33	0.43	.013	.017
C	0.15	0.25	.006	.010
D/E	20.32 BSC		.800 BSC	
D1/E1	23.65	24.10	.931	.949
D2/E2	24.89	25.40	.980	1.000
e	1.27 BSC		.050 BSC	
L1	0.51	1.14	.020	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outlines	A, B, M, 9	Case outlines	A, B, M, 9	Case outlines	A, B, M, 9	Case outlines	A, B, M, 9
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

FIGURE 2. Terminal connections.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	T, U, X	Case outline	T, U, X	Case outline	T, U, X	Case outline	T, U, X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A12	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/03	39	NC	56	I/O31
6	A15	23	I/015	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	A18	45	V_{CC}	62	A2
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

FIGURE 2. Terminal connections - Continued.

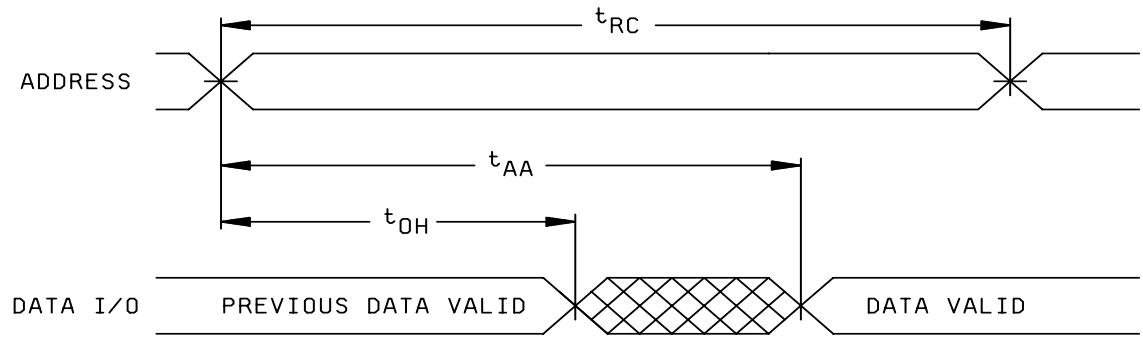
Device types	All	Device types	All	Device types	All	Device types	All
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections - Continued.

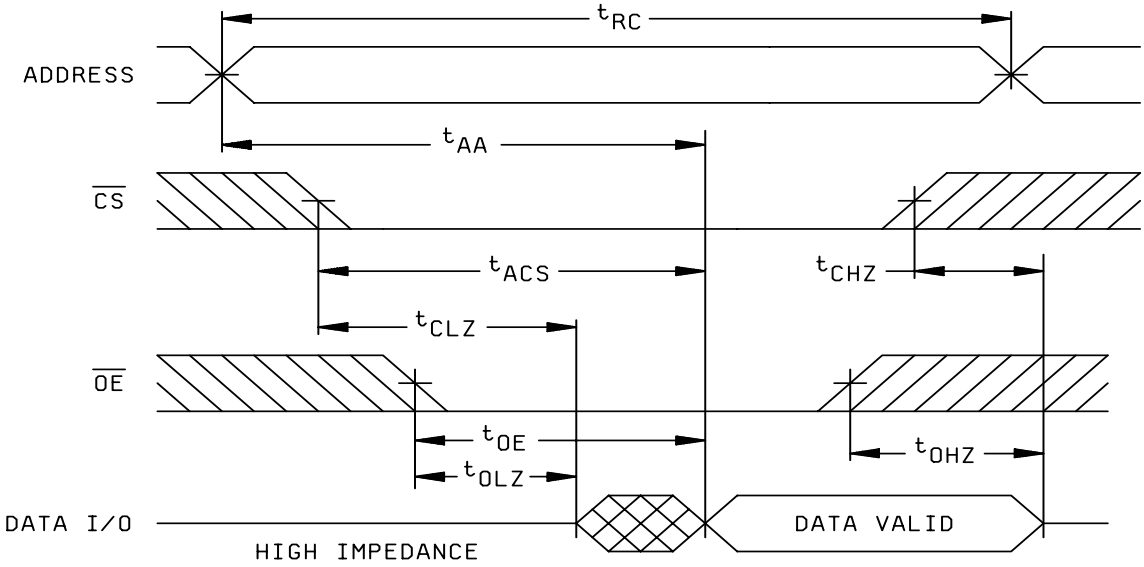
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write

NOTES:
1. V_{IH} = High logic level
2. V_{IL} = Low logic level
3. X = Do not care (either high or low)
4. High Z = High impedance state

FIGURE 3. Truth table.

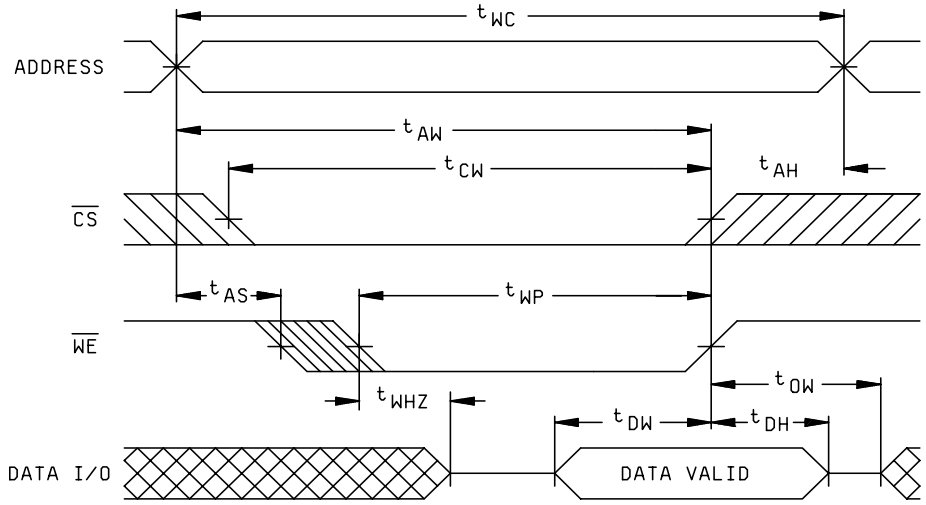


READ CYCLE 1 ($\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

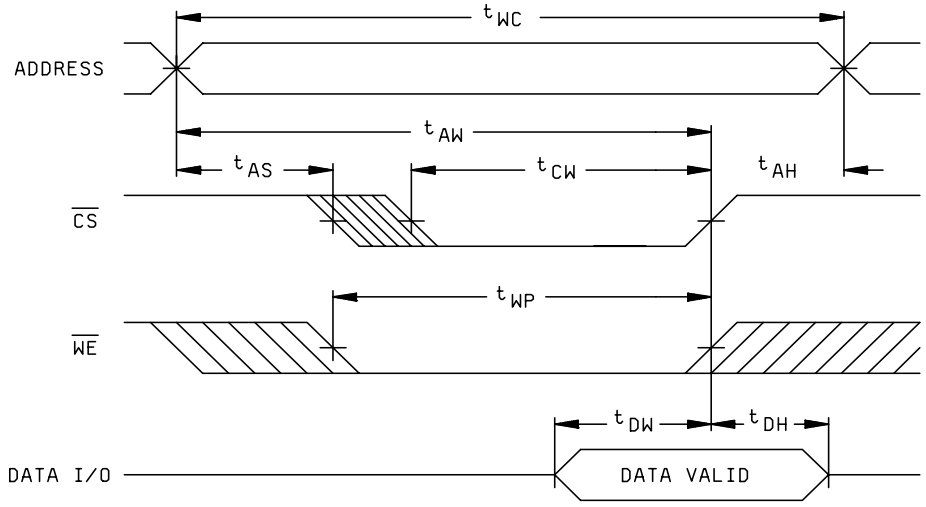


READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIGURE 4. Read cycle timing diagram.



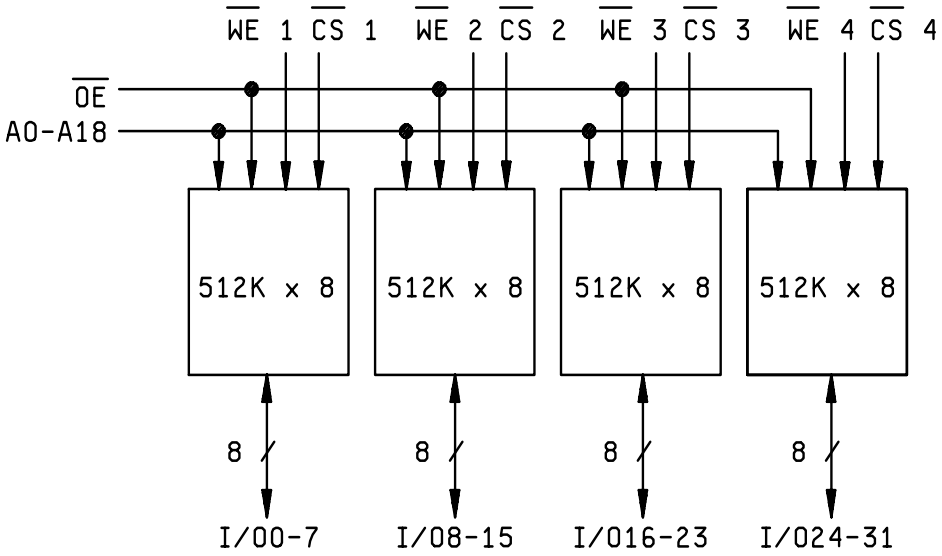
WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.

Case outlines A, B, M, T, U, X, and 9.



Case outline Y.

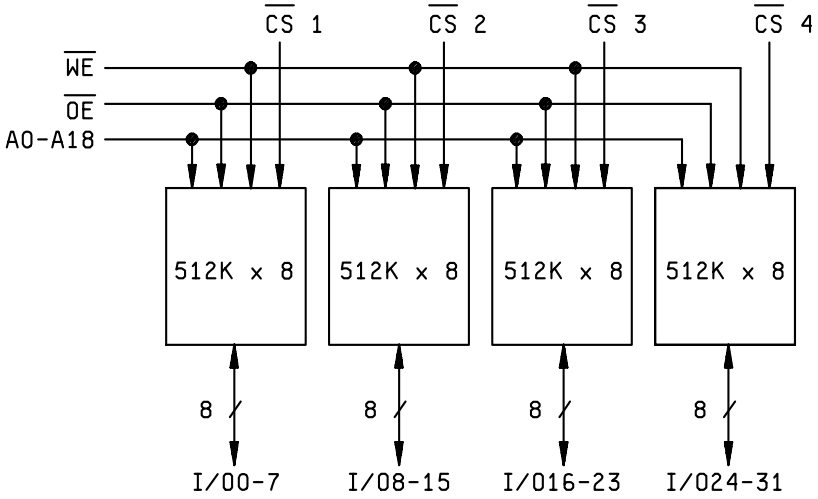
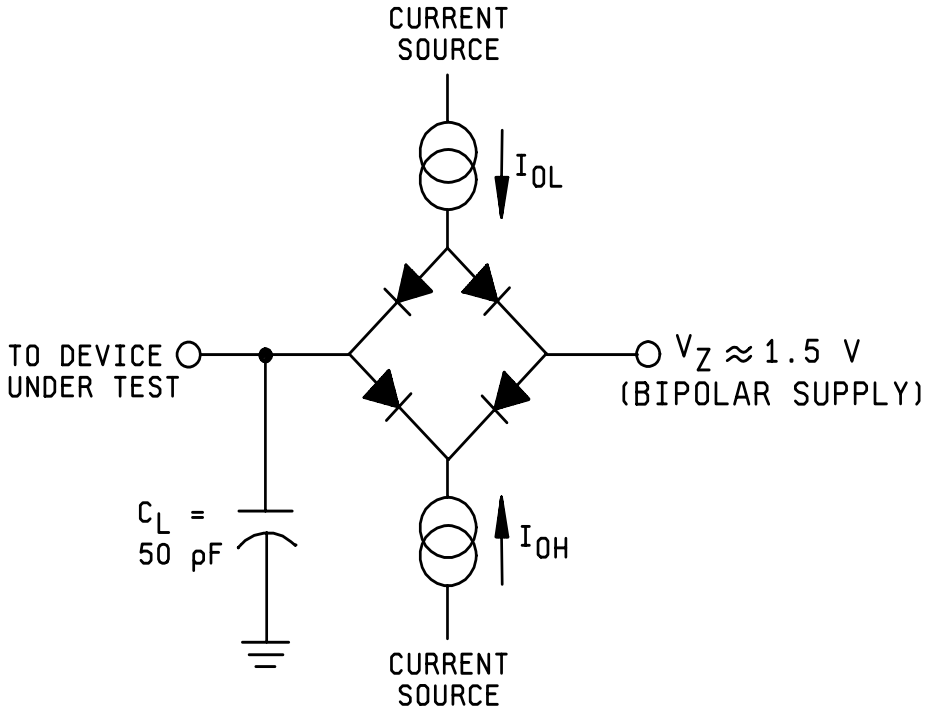


FIGURE 6. Block diagram(s).



Parameter	Typical	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from -2 V to +7 V
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical Parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable.

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation hardness assurance (RHA) insepction. RHA inspection is currently not applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.