

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

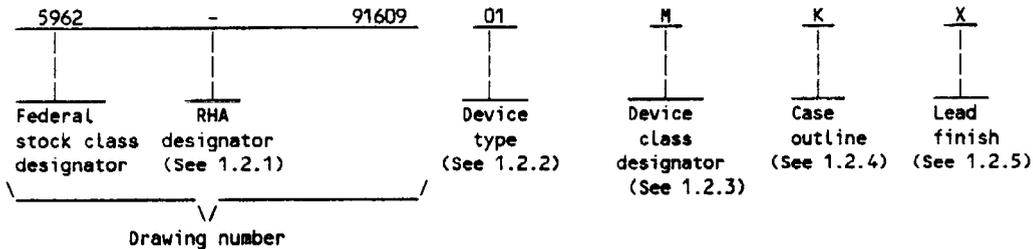
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<b>PMIC N/A</b>	PREPARED BY <i>Marcia B Kelleher</i>	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		
	CHECKED BY <i>James L. Polking</i>	MICROCIRCUITS, DIGITAL, ADVANCED CMOS, 8-BIT DIAGNOSTIC REGISTER, MONOLITHIC SILICON		
<b>STANDARDIZED                  MILITARY                  DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	APPROVED BY 	SIZE      CAGE CODE      5962-91609 A            67268		
	DRAWING APPROVAL DATE 92-04-07	SHEET      1                      OF      22		
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1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54ACT818	8-bit diagnostic register, TTL compatible inputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

<u>Outline letter</u>	<u>Case outline</u>
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-lead, .460" x .460" x .100"), square chip carrier package

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1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range	- - - - -	-0.5 V dc to +7.0 V dc
DC input voltage	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage	- - - - -	-0.5 V dc to $V_{CC} + 0.5$ V dc
Clamp diode current	- - - - -	$\pm 20$ mA
DC output current (per pin)	- - - - -	$\pm 50$ mA
DC $V_{CC}$ or GND current (per pin)	- - - - -	$\pm 450$ mA
Storage temperature range	- - - - -	-65°C to +150°C
Maximum power dissipation ( $P_D$ )	- - - - -	500 mW
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Thermal resistance, junction-to-case ( $\Theta_{JC}$ )	- - - - -	See MIL-M-38510, appendix C
Junction temperature ( $T_J$ ) 2/	- - - - -	+175°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ )	- - - - -	+4.5 V dc to +5.5 V dc
Input voltage range	- - - - -	0.0 V dc to $V_{CC}$
Output voltage range	- - - - -	0.0 V dc to $V_{CC}$
Case operating temperature range ( $T_C$ )	- - - - -	-55°C to +125°C
Input rise or fall times:		
$V_{CC} = 4.5$ V, 5.5 V	- - - - -	8 ns/V
Minimum setup time, Dn to PCLK ( $t_{s1}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	4.0 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	6.0 ns
Minimum setup time, MODE to PCLK ( $t_{s2}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	4.5 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	6.0 ns
Minimum setup time, Yn to DCLK ( $t_{s3}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	2.5 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	2.5 ns
Minimum setup time, MODE to DCLK ( $t_{s4}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	4.0 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	4.5 ns
Minimum setup time, SDI to DCLK ( $t_{s5}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	3.5 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	4.5 ns
Minimum setup time, DCLK to PCLK ( $t_{s6}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	9.0 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	11.5 ns
Minimum setup time, PCLK to DCLK ( $t_{s7}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	11.0 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	12.5 ns
Minimum hold time, Dn to PCLK ( $t_{h1}$ ):		
$T_C = +25^\circ\text{C}$ , $V_{CC} = 4.5$ V	- - - - -	1.0 ns
$T_C = -55^\circ\text{C}$ , +125°C, $V_{CC} = 4.5$ V	- - - - -	1.0 ns

1/ Unless otherwise specified, all voltages are referenced to GND.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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Minimum hold time, MODE to PCLK ( $t_{h2}$ ):	0.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	0.0 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	0.0 ns
Minimum hold time, Yn to DCLK ( $t_{h3}$ ):	1.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.5 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.5 ns
Minimum hold time, MODE to DCLK ( $t_{h4}$ ):	1.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.0 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.0 ns
Minimum hold time, SDI to DCLK ( $t_{h5}$ ):	1.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.0 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	1.0 ns
Minimum PCLK pulse width, high, low ( $t_{w1}$ ):	3.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	3.5 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	3.5 ns
Minimum DCLK pulse width, high, low ( $t_{w2}$ ):	3.0 ns
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	3.0 ns
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	3.0 ns
Maximum clock frequency ( $f_{max}$ ):	100 MHz
$T_C = +25^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	100 MHz
$T_C = -55^\circ\text{C}, +125^\circ\text{C}, V_{CC} = 4.5\text{ V}$ - - - - -	100 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) - - - - XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

3/ Values will be added when they become available.

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HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

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3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 40 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein. Interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High level output voltage Y0-Y7 outputs 1/	V <sub>OH1</sub>	V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OH</sub> = -50 μA	V <sub>CC</sub> = 4.5 V	1, 2, 3	4.4	V
					V <sub>CC</sub> = 5.5 V	
		V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OH</sub> = -24 mA	V <sub>CC</sub> = 4.5 V	1, 2, 3	3.7	
					V <sub>CC</sub> = 5.5 V	4.7
V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OH</sub> = -50 mA	V <sub>CC</sub> = 5.5 V	1, 2, 3	3.85			
High level output voltage 00-07, SD0 outputs 1/	V <sub>OH2</sub>	V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OH</sub> = -8 mA	V <sub>CC</sub> = 4.5 V	1, 2, 3	3.7	V
					V <sub>CC</sub> = 5.5 V	
		V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = -32 mA	V <sub>CC</sub> = 5.5 V	1, 2, 3	3.85	
Low level output voltage Y0-Y7 outputs 1/	V <sub>OL1</sub>	V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = 50 μA	V <sub>CC</sub> = 4.5 V	1, 2, 3		0.1
					V <sub>CC</sub> = 5.5 V	0.1
		V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = 24 mA	V <sub>CC</sub> = 4.5 V	1, 2, 3		0.5
					V <sub>CC</sub> = 5.5 V	0.5
V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = 50 mA	V <sub>CC</sub> = 5.5 V	1, 2, 3		1.65		
Low level output voltage 00-07, SD0 outputs 1/	V <sub>OL2</sub>	V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = 8 mA	V <sub>CC</sub> = 4.5 V	1, 2, 3		0.5
					V <sub>CC</sub> = 5.5 V	0.5
		V <sub>IN</sub> = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, I <sub>OL</sub> = 32 mA	V <sub>CC</sub> = 5.5 V	1, 2, 3		1.65

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>c</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High level input voltage ②/	V <sub>IH</sub>		V <sub>CC</sub> = 4.5 V	1, 2, 3	2.0	V
					V <sub>CC</sub> = 5.5 V	
Low level input voltage ②/	V <sub>IL</sub>		V <sub>CC</sub> = 4.5 V	1, 2, 3	0.8	V
					V <sub>CC</sub> = 5.5 V	
Input leakage current, SDI, DCLK, MODE, PCLK, OEY	I <sub>IL</sub>	V <sub>IN</sub> = 0.0 V	V <sub>CC</sub> = 5.5 V	1, 2, 3	-10.0	μA
	I <sub>IH</sub>	V <sub>IN</sub> = 5.5 V			+10.0	
Three-state leakage current, Dn, Yn	I <sub>OZH</sub>	OEY = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, all other inputs at V <sub>CC</sub> or GND, V <sub>OUT</sub> = 5.5 V	V <sub>CC</sub> = 5.5 V	1, 2, 3	+10.0	μA
	I <sub>OZL</sub>	OEY = V <sub>IH</sub> minimum or V <sub>IL</sub> maximum, all other inputs at V <sub>CC</sub> or GND, V <sub>OUT</sub> = 0.0 V			-10.0	
Maximum I <sub>CC</sub> /input ③/ current, SDI, Dn, DCLK, MODE, OEY	ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.0 V, V <sub>IH</sub> = V <sub>CC</sub> - 2.1 V		1, 2, 3	1.6	mA
Quiescent current	I <sub>CCH</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 5.5 V		1, 2, 3	160	μA
	I <sub>CCL</sub>				160	
	I <sub>CCZ</sub>				160	
Input capacitance	C <sub>IN</sub>	See 4.4.1c		4	8.0	pF
Output capacitance	C <sub>OUT</sub>	See 4.4.1c		4	15.0	pF
Input/output capacitance	C <sub>IO</sub>	See 4.4.1c		4	15.0	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit	
				Min	Max		
Power dissipation capacitance 4/	C <sub>PD</sub>	See 4.4.1c	4		110	pF	
Functional tests		Tested at V <sub>CC</sub> = 4.5 V and repeated at V <sub>CC</sub> = 5.5 V, for all inputs V <sub>IN</sub> = 2.4 V or 0.4 V, see 4.4.1d	7, 8				
Propagation delay time, PCLK to Yn 5/	t <sub>PHL1</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	8.0	ns
	t <sub>PLH1</sub>				1.0	8.5	
	t <sub>PHL1</sub>			10, 11	1.0	10.0	
	t <sub>PLH1</sub>				1.0	10.0	
Propagation delay time, MODE to SDO 5/	t <sub>PHL2</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	10.0	ns
	t <sub>PLH2</sub>				1.0	11.0	
	t <sub>PHL2</sub>			10, 11	1.0	12.0	
	t <sub>PLH2</sub>				1.0	13.5	
Propagation delay time, SDI to SDO 5/	t <sub>PHL3</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	9.5	ns
	t <sub>PLH3</sub>				1.0	10.0	
	t <sub>PHL3</sub>			10, 11	1.0	11.5	
	t <sub>PLH3</sub>				1.0	12.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit	
				Min	Max		
Propagation delay time, DCLK to S00  5/	t <sub>PHL4</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	11.5	ns
	t <sub>PLH4</sub>				1.0	12.0	
	t <sub>PHL4</sub>			10, 11	1.0	14.0	
	t <sub>PLH4</sub>				1.0	15.5	
Output enable time, OEY to Yn  5/	t <sub>PZH1</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	9.5	ns
	t <sub>PZL1</sub>				1.0	10.5	
	t <sub>PZH1</sub>			10, 11	1.0	11.0	
	t <sub>PZL1</sub>				1.0	12.0	
Output disable time, OEY to Yn  5/	t <sub>PHZ1</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	10.5	ns
	t <sub>PLZ1</sub>				1.0	8.5	
	t <sub>PHZ1</sub>			10, 11	1.0	12.0	
	t <sub>PLZ1</sub>				1.0	10.0	
Output enable time, DCLK to Dn  5/	t <sub>PZH2</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	V <sub>CC</sub> = 4.5 V	9	1.0	11.0	ns
	t <sub>PZL2</sub>				1.0	11.5	
	t <sub>PZH2</sub>			10, 11	1.0	13.5	
	t <sub>PZL2</sub>				1.0	14.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output disable time, DCLK to Dn  5/	t <sub>PHZ2</sub>	C <sub>L</sub> = 50 pF minimum, R <sub>L</sub> = 500Ω, See figure 4	9	1.0	12.0	ns
	t <sub>PLZ2</sub>			1.0	10.5	
	t <sub>PHZ2</sub>		10, 11	1.0	13.5	
	t <sub>PLZ2</sub>			1.0	12.0	

- 1/ V<sub>OH</sub> and V<sub>OL</sub> tests will be tested at V<sub>CC</sub> = 4.5 V. All other voltages are guaranteed, but not tested. Limits shown apply to operation at V<sub>CC</sub> = 5.0 V ±0.5 V. Transmission driving tests are performed at V<sub>CC</sub> = 5.5 V with a 2 ms duration maximum.
- 2/ V<sub>IH</sub> and V<sub>IL</sub> tests are guaranteed by the V<sub>OH</sub> and V<sub>OL</sub> tests.
- 3/ Delta I<sub>CC</sub> (max)/pin ≤ 1.6 mA (preferred method), or delta I<sub>CC</sub>/package ≤ 1.6 mA x the number of input pins/package where delta I<sub>CC</sub> (max)/data pin ≤ 1.6 mA and delta I<sub>CC</sub> (max)/control pin ≤ 3.0 mA (alternate method).
- 4/ Power dissipation capacitance (C<sub>PD</sub>), determines the dynamic power consumption, P<sub>D</sub> = (C<sub>PD</sub> + C<sub>L</sub>) (V<sub>CC</sub> x V<sub>CC</sub>)f + I<sub>CC</sub> (V<sub>CC</sub>), and the dynamic current consumption (I<sub>S</sub>) is, I<sub>S</sub> = (C<sub>PD</sub> + C<sub>L</sub>) V<sub>CC</sub> f + I<sub>CC</sub>.
- 5/ AC limits at 5.5 V V<sub>CC</sub> are equal to limits at 4.5 V V<sub>CC</sub> and guaranteed by testing at 4.5 V V<sub>CC</sub>. Minimum ac guaranteed for 5.5 V V<sub>CC</sub> by guardbanding 4.5 V V<sub>CC</sub> limits to 1.5 ns (minimum).

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

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Device type	01	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	OEY	NC
2	DCLK	OEY
3	D0	DCLK
4	D1	D0
5	D2	D1
6	D3	D2
7	D4	D3
8	D5	NC
9	D6	D4
10	D7	D5
11	SDI	D6
12	GND	D7
13	PCLK	SDI
14	SDO	GND
15	Y7	NC
16	Y6	PCLK
17	Y5	SDO
18	Y4	Y7
19	Y3	Y6
20	Y2	Y5
21	Y1	Y4
22	Y0	NC
23	MODE	Y3
24	V <sub>CC</sub>	Y2
25	---	Y1
26	---	Y0
27	---	MODE
28	---	V <sub>CC</sub>

NC = No connection

Pin names	Description
D <sub>0</sub> -D <sub>7</sub>	Data inputs
SDI	Serial data input
DCLK	Diagnostics clock
MODE	Control input
PCLK	Pipeline register clock
OEY	Output enable input
SDO	Serial data output
Y <sub>0</sub> -Y <sub>7</sub>	Data outputs

FIGURE 1. Terminal connections.

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Inputs					Outputs		Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic register	Pipeline register	
X	L	$\overline{\text{L}}$	X	S7	S1<S1 - 1, S0<SDI	N/A	Serial shift; D7-D0 disabled
X	L	X	$\overline{\text{L}}$	S7	N/A	P1<D1	Normal load pipeline register
L	H	$\overline{\text{L}}$	X	L	S1<Y1	N/A	Load diagnostic register from Y; D1 disabled
X	H	X	$\overline{\text{L}}$	SDI	N/A	P1<S1	Load pipeline register from diagnostic register
H	H	$\overline{\text{L}}$	X	H	Hold	N/A	Hold diagnostic register; D1 enabled

H = HIGH voltage level  
 L = LOW voltage level  
 X = Immaterial  
 $\overline{\text{L}}$  = LOW-to-HIGH clock transition

FIGURE 2. Truth table.

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8-BIT DIAGNOSTIC REGISTER

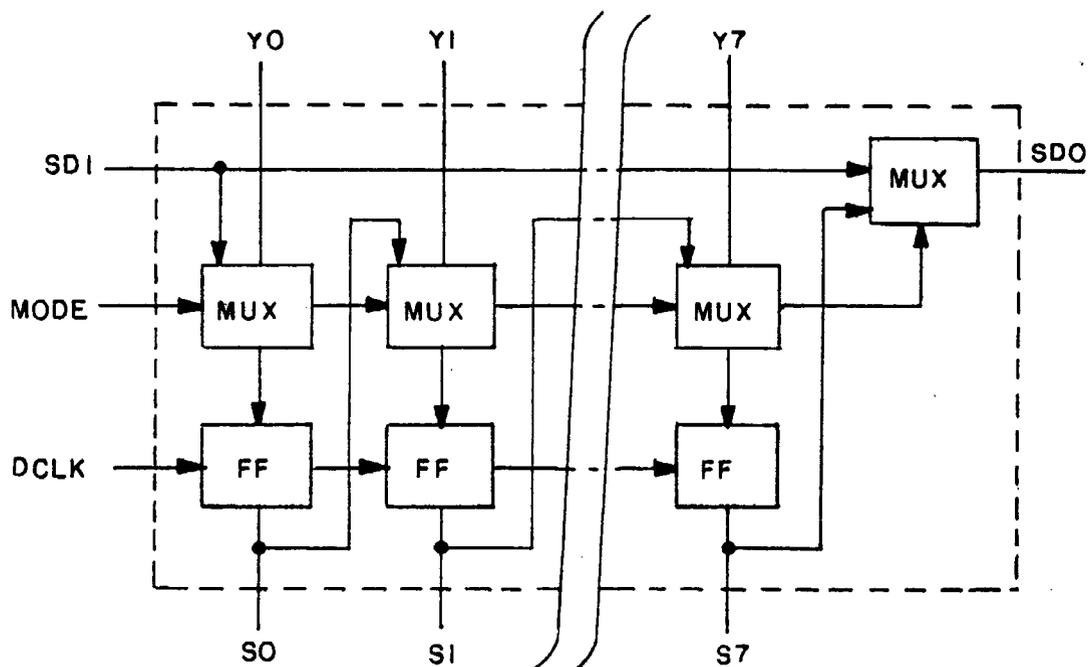


FIGURE 3. Block diagram.

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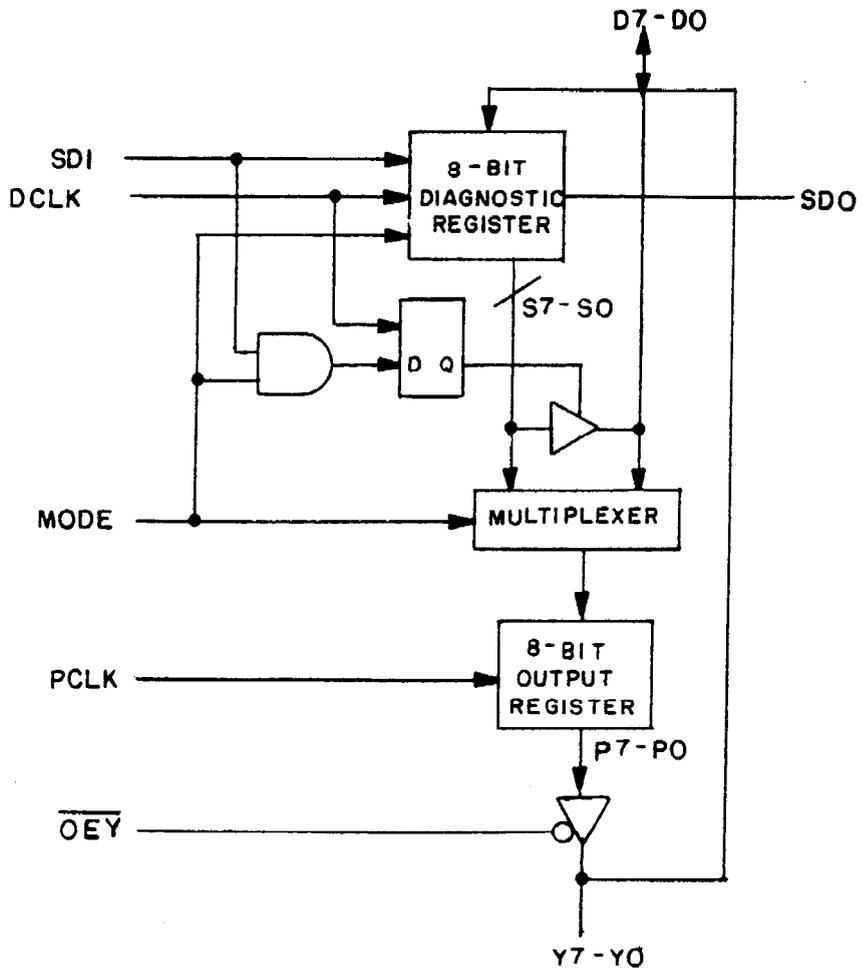


FIGURE 3. Block diagram - Continued.

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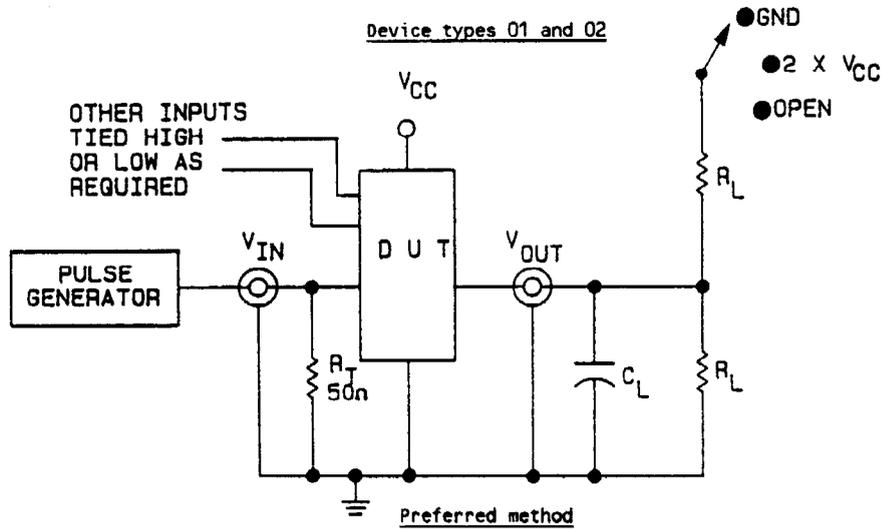
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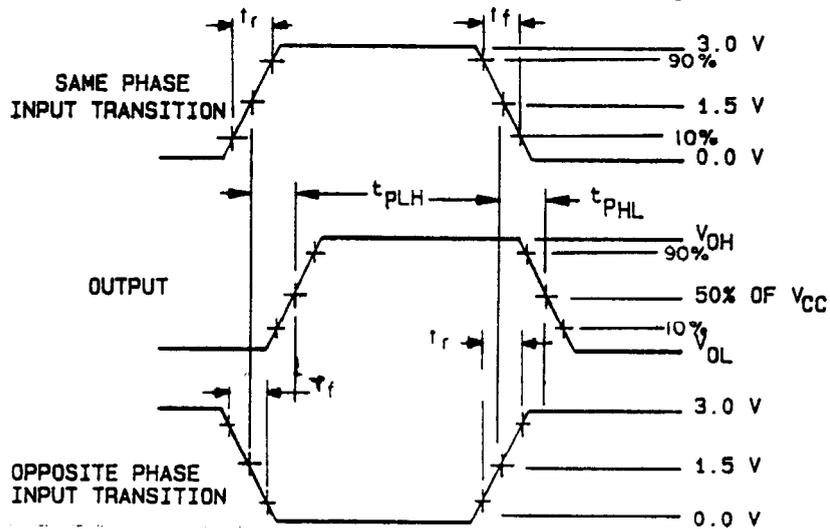


$GND = t_{PHZ}$  and  $t_{PZH}$   
 $2 \times V_{CC} = t_{PLZ}$  and  $t_{PZL}$   
 $Open = t_{PLH}$  and  $t_{PHL}$

Alternate method

$Open = t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLH}$ , and  $t_{PHL}$   
 $2 \times V_{CC} = t_{PLZ}$  and  $t_{PZL}$

NOTE:  $R_T = 50\Omega$ ,  $C_L = 50$  pF minimum, includes probe and jig capacitance,  $R_L = 500\Omega$ , or equivalent.



NOTE:  $t_r$ ,  $t_f \leq 3.0$  ns, 10 percent to 90 percent, or equivalent.

FIGURE 4. Test circuit and switching waveforms.

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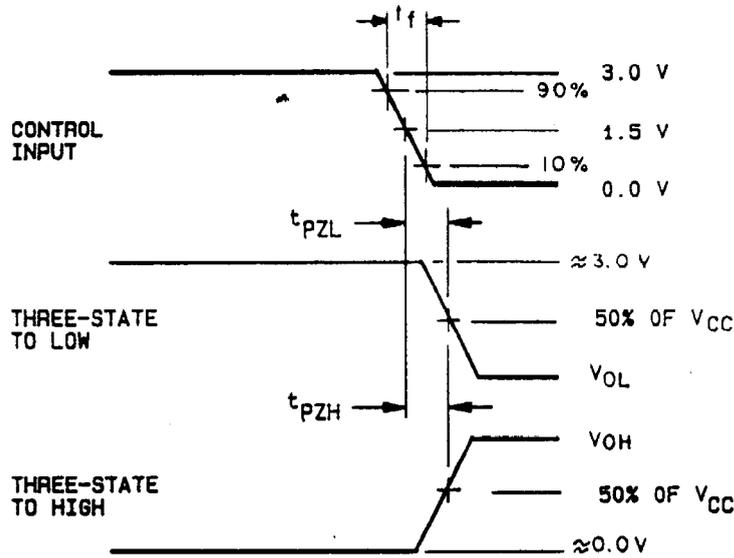
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ENABLE TIMES



DISABLE TIMES

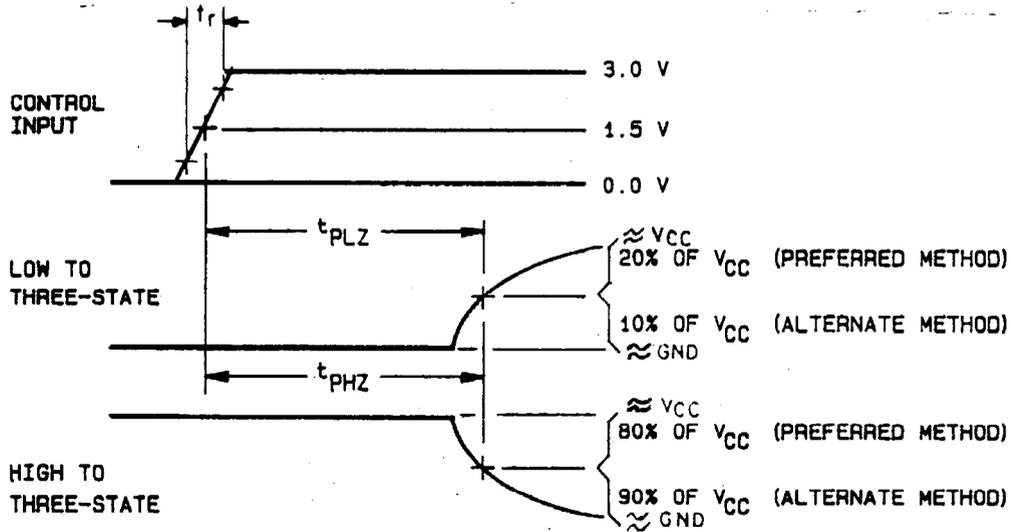


FIGURE 4. Test circuit and switching waveforms - Continued.

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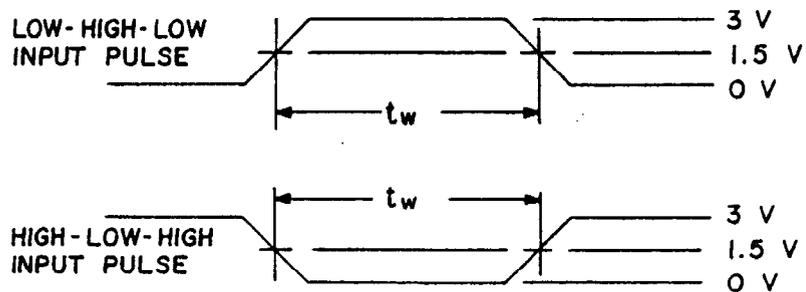
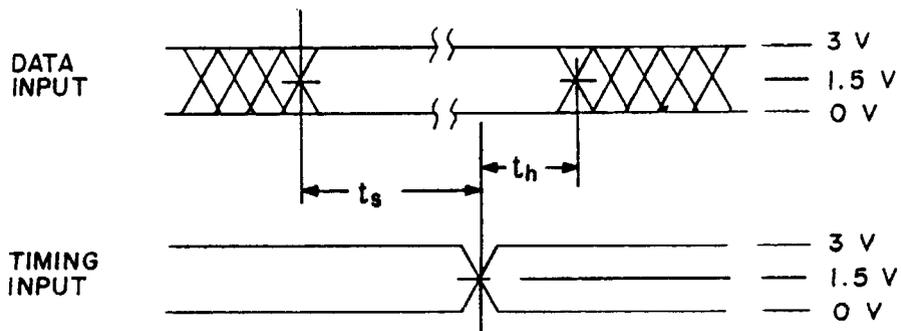


FIGURE 4. Test circuit and switching waveforms - Continued.

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4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$ ,  $C_{IN/OUT}$  and  $C_{PD}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the input terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.
- d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1	1	1
Final electrical parameters (see 4.2)	1/ 1,2,3,7, 8,9	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 7,8,9,10,11	1,2,3,4, 7,8,9,10,11	1,2,3,4, 7,8,9,10,11	1,2,3,4, 7,8,9,10,11	1,2,3,4, 7,8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3, 9,10,11		1,2,3, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3		1,2,3	
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

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4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table IIA herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.
- d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5$  percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

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6.5 Symbols, definitions, and functional descriptions.

GND - - - - - Ground zero voltae potential.  
 I<sub>CC</sub> - - - - - Quiescent supply current.  
 I<sub>IL</sub> - - - - - Input current low.  
 I<sub>IH</sub> - - - - - Input current high.  
 T<sub>C</sub> - - - - - Case temperature.  
 V<sub>CC</sub> - - - - - Positive supply voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

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