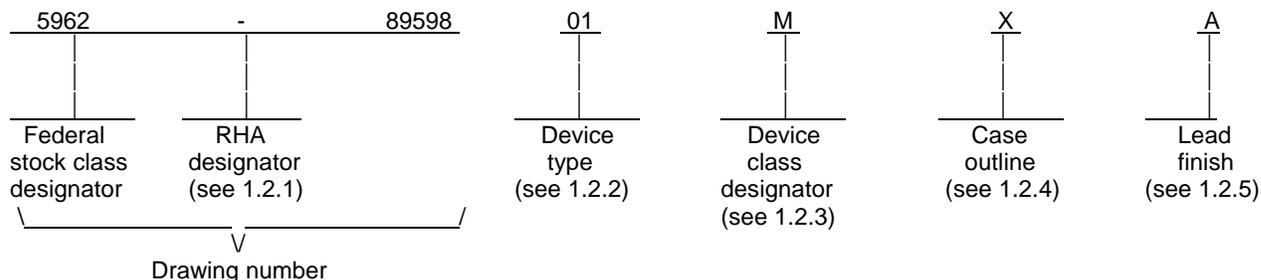


REVISIONS																					
LTR	DESCRIPTION										DATE (YR-MO-DA)					APPROVED					
H	Add device type 41. Make corrections to case outline N, dimension b. Add vendor CAGE 65786 as source of supply for device type 41. Update boilerplate. Editorial changes throughout.										97-03-26					Raymond Monnin					
J	Add device types 42, 43, 44, 45, and 46. Editorial changes to pages 1, 3, 7-15. Update boilerplate. ksr										98-03-03					Raymond Monnin					
K	Added provisions to accommodate radiation-hardened devices. Added device type 47 to drawing. glg										00-03-01					Raymond Monnin					
L	Corrected case outline 8 Figure 1 to show correct numbering of terminals. Corrected Figure 2 Terminal connections. Corrected the case outline Y Figure 1 to show the proper distance of E and E1. Added note to Case outline Y Figure 1, to allow for bottom brazed package as an alternative style to the side brazed package . Update boilerplate. Editorial changes throughout. ksr										00-12-08					Raymond Monnin					
M	Changed the minimum value for the Q dimension on package T from 0.026 to 0.020 and removed footnote 12. Editorial changes throughout.. ksr										02-12-19					Raymond Monnin					
N	Added device type 48 to drawing. ksr										03-08-12					Raymond Monnin					
REV	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52			
REV	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
REV STATUS OF SHEETS				REV			N	N	N	N	N	N	N	N	N	N	N	N	N	N	
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY Kenneth S. Rice					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsccl.dla.mil												
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Raymond Monnin																	
				APPROVED BY Michael A. Frye																	
				DRAWING APPROVAL DATE 89-04-21																	
				REVISION LEVEL N																	
					SIZE A	CAGE CODE 67268			5962-89598												
					SHEET 1 OF 52																

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>Access time</u>
01		128K x 8 low power CMOS SRAM	120 ns
02		128K x 8 low power CMOS SRAM	100 ns
03		128K x 8 low power CMOS SRAM	85 ns
04		128K x 8 low power CMOS SRAM	70 ns
05		128K x 8 low power CMOS SRAM	120 ns
06		128K x 8 low power CMOS SRAM	100 ns
07		128K x 8 low power CMOS SRAM	85 ns
08		128K x 8 low power CMOS SRAM	70 ns
09		128K x 8 low power CMOS SRAM	55 ns
10		128K x 8 low power CMOS SRAM	45 ns
11		128K x 8 low power CMOS SRAM	35 ns
12		128K x 8 low power CMOS SRAM	25 ns
13		128K x 8 low power CMOS SRAM dual CE	120 ns
14		128K x 8 low power CMOS SRAM dual CE	100 ns
15		128K x 8 low power CMOS SRAM dual CE	85 ns
16		128K x 8 low power CMOS SRAM dual CE	70 ns
17		128K x 8 low power CMOS SRAM dual CE	55 ns
18		128K x 8 low power CMOS SRAM dual CE	45 ns
19		128K x 8 low power CMOS SRAM dual CE	35 ns
20		128K x 8 low power CMOS SRAM dual CE	25 ns
21		128K x 8 low power CMOS SRAM dual CE	20 ns
22		128K x 8 standard power CMOS SRAM	120 ns
23		128K x 8 standard power CMOS SRAM	100 ns
24		128K x 8 standard power CMOS SRAM	85 ns
25		128K x 8 standard power CMOS SRAM	70 ns
26		128K x 8 standard power CMOS SRAM	55 ns
27		128K x 8 standard power CMOS SRAM	45 ns
28		128K x 8 standard power CMOS SRAM	35 ns
29		128K x 8 standard power CMOS SRAM	25 ns
30		128K x 8 standard power CMOS SRAM dual CE	120 ns

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 2

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>Access time</u>
31		128K x 8 standard power CMOS SRAM dual CE	100 ns
32		128K x 8 standard power CMOS SRAM dual CE	85 ns
33		128K x 8 standard power CMOS SRAM dual CE	70 ns
34		128K x 8 standard power CMOS SRAM dual CE	55 ns
35		128K x 8 standard power CMOS SRAM dual CE	45 ns
36		128K x 8 standard power CMOS SRAM dual CE	35 ns
37		128K x 8 standard power CMOS SRAM dual CE	25 ns
38		128K x 8 standard power CMOS SRAM dual CE	20 ns
39		128K x 8 standard power CMOS SRAM	20 ns
40		128K x 8 low power CMOS SRAM	20 ns
41		128K x 8 standard power CMOS SRAM dual CE	15 ns
42		128K x 8 low power CMOS SRAM	70 ns
43		128K x 8 standard power CMOS SRAM	70 ns
44		128K x 8 standard power CMOS SRAM	15 ns
45		128K x 8 standard power CMOS SRAM dual CE	12 ns
46		128K x 8 standard power CMOS SRAM	12 ns
47		128K x 8 very low power CMOS SRAM	30 ns
48		128K x 8 low power CMOS SRAM	15 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDIP1-T32 or CDIP2-T32	32	dual-in-line
Y <u>2/</u>	See figure 1	32	SOJ package
Z	See figure 1	32	dual-in-line
U	See figure 1	32	rectangular chip carrier
T	See figure 1	32	flat pack
N	See figure 1	32	rectangular chip carrier
M	CQCC1-N32	32	rectangular chip carrier
9	See figure 1	32	J-leaded rectangular chip carrier
8	See figure 1	32	zig-zag in-line
7	See figure 1	32	SOJ package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 3/ 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}).....	-0.5 V dc to $V_{CC}+0.5$ V dc <u>5/</u>
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC}+0.5$ V dc <u>5/</u>
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds).....	+260°C

- 1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
- 2/ A bottom brazed option for this package now exists (See figure 1, case outline Y NOTE:). Customers may specify in the purchase order to negate the option as acceptable for their use.
- 3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 4/ All voltages referenced to V_{SS} (V_{SS} = ground) unless otherwise specified.
- 5/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

3

1.3 Absolute maximum ratings - continued. 3/ 4/

Thermal resistance, junction-to-case (θ_{JC}):	
Case M	See MIL-STD-1835
Cases X, Y, Z, U, and 7	11°C/W <u>6/</u>
Cases T, N, and 9	10°C/W <u>6/</u>
Case 8	16°C/W <u>6/</u>
Output voltage applied in high Z state	-0.5 V dc to $V_{CC}+0.5$ V dc
Maximum power dissipation, (P_D)	1.0 W
Maximum junction temperature (T_J)	+150°C <u>7/</u>

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage range (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.2 V dc to $V_{CC} + 0.5$ V dc
Low level input voltage range (V_{IL})	-0.5 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- 3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 4/ All voltages referenced to V_{SS} (V_{SS} = ground) unless otherwise specified.
- 6/ When the θ_{JC} for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
- 7/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 4

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 5

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Substitution. Substitution data shall be as indicated in appendix B herein.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 6

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level input current	I _{IH}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	1, 2, 3	All		10	μA
		M,D,P	1 <u>1/</u>			<u>2/</u>	
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.0 V	1, 2, 3	All	-10		μA
		M,D,P	1 <u>1/</u>		<u>2/</u>		
High impedance output leakage current	I _{OZH}	V _{CC} = 5.5 V, V _O = 5.5 V V _{IL} = 0.0 V, V _{IH} = 5.0 V V _{IH} ≤ \overline{OE} ≤ V _{CC}	1, 2, 3	All		10	μA
		M,D,P	1 <u>1/</u>			<u>2/</u>	
	I _{OZL}	V _{CC} = 5.5 V, V _O = 0.0 V V _{IL} = 0.0 V, V _{IH} = 5.0 V V _{IH} ≤ \overline{OE} ≤ V _{CC}	1, 2, 3	All	-10		
		M,D,P	1 <u>1/</u>		<u>2/</u>		
Output high voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = 4.5 V V _{IH} = 2.2 V, V _{IL} = 0.8 V	1, 2, 3	01-41, 47,48	2.4		V
			M,D,P		1 <u>1/</u>	<u>2/</u>	
		I _{OH} = -1.0 mA, V _{CC} = 4.5 V V _{IH} = 2.2 V, V _{IL} = 0.8 V		42- 46	2.4		
			M,D,P		1 <u>1/</u>	<u>2/</u>	
Output low voltage	V _{OL}	I _{OL} = 8.0 mA, V _{CC} = 4.5 V V _{IH} = 2.2 V, V _{IL} = 0.8 V	1, 2, 3	01-41, 47,48		0.4	V
			M,D,P		1 <u>1/</u>		
		I _{OL} = 2.1 mA, V _{CC} = 4.5 V V _{IH} = 2.2 V, V _{IL} = 0.8 V		42- 46		0.4	
			M,D,P		1 <u>1/</u>	<u>2/</u>	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 7

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I _{CC1}	V _{CC} = 5.5 V, $\overline{CE} = V_{IL}$ max \overline{OE} , \overline{WE} , and CE ₂ = V _{IH} f = 1/t _{AVAV} min	1, 2, 3	01-04, 11,19, 26,27, 34,35, 42		125	mA
				05, 06, 13, 14		100	
				07, 08, 15, 16, 22, 23, 30, 31		110	
				09, 10, 17, 18		115	
				24, 25, 32, 33, 43		120	
				12,20, 47		130	
				28, 36		135	
				21, 29, 37, 39, 40,48		140	
				38		150	
				41		180	
				44-46		250	
		M,D,P	1 <u>1</u> /	All		<u>2</u> /	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

8

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Standby supply current TTL	I _{CC2}	V _{CC} = 5.5 V, $\overline{CE} = V_{IH}$ CE ₂ = V _{IL} , f = 0 Hz	1, 2, 3	47		2	mA
				01-04, 42		10	
				05-40, 43,48		25	
				41		40	
				44-46		60	
	M,D,P	1 1/	All		2/		
Standby supply current CMOS	I _{CC3}	V _{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V Inputs = V _{IH} or V _{IL} , f = 0	1, 2, 3	47		0.3	mA
				42		1	
				01-04, 40,43,48		5	
				05-39, 41		10	
				44-46		15	
	M,D,P	1 1/	All		2/		
Data retention current	I _{CC4}	V _{CC} = 2.0 V, f = 0 $\overline{CE} \geq V_{CC} - 0.2$ V, all other inputs = 0.2 V or V _{CC} - 0.2 V	1, 2, 3	01-04		2	mA
				05-21		1	
				40,48		750	μA
				42		400	
				47		150	
	M,D,P	1 1/	All		2/		
Input capacitance 3/ (A0 - A16)	C _{IN}	V _{IN} = 0 V, f = 1.0 MHz T _C = +25°C, see 4.4.1e	4	01-38, 41-47		12	pF
				39, 40,48		5	
Input capacitance 3/ (\overline{CE} , \overline{WE} , \overline{OE})	C _{CLK}	V _{OUT} = 0 V, f = 1.0 MHz T _C = +25°C, see 4.4.1e	4	01-38, 41-47		20	pF
				39, 40,48		5	
Output capacitance 3/	C _{OUT}	V _{OUT} = 0 V, f = 1.0 MHz T _C = +25°C, see 4.4.1e	4	01-38, 41-47		14	pF
				39, 40,48		5	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 9

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional tests <u>4/</u>		See 4.4.1c	7, 8A, 8B	All			
			M,D,P		7 <u>1/</u>	<u>2/</u>	
Read cycle time	t _{AVAV}	See figure 4, as applicable <u>5/ 6/</u>	9, 10, 11	01,05, 13,22,30	120		ns
				02,06, 14,23,31	100		
				03,07,15, 24,32	85		
				04,08,16, 25,33,42, 43	70		
				09,17, 26,34	55		
				10,18, 27,35	45		
				11,19, 28,36	35		
				47	30		
				12,20, 29,37	25		
				21,38-40	20		
				41,44,48	15		
				45,46	12		
					M,D,P	9 <u>1/</u>	All

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 10

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address access time	t _{AVQV}	See figure 4, as applicable	9, 10, 11	01,05, 13,22, 30		120	ns
				02,06, 14,23, 31		100	
				03,07, 15,24, 32		85	
				04,08, 16,25, 33,42, 43		70	
				09,17, 26,34		55	
				10,18, 27,35		45	
				11,19, 28,36		35	
				47		30	
				12,20, 29,37		25	
				21, 38-40		20	
				41,44,48		15	
				45,46		12	
					M,D,P		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 11

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip enable access time	t _{ELQV}	See figure 4, as applicable	9, 10, 11	01,05, 13,22,30		120	ns
				02,06, 14,23,31		100	
				03,07, 15,24,32		85	
				04,08, 16,25, 33,42,43		70	
				09,17, 26,34		55	
				10,18, 27,35		45	
				11,19, 28,36		35	
				47		30	
				12,20, 29,37		25	
				21,38-40		20	
				41,44,48		15	
				45,46		12	
					M,D,P	9 1/	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 12

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output enable to output valid	t _{OLQV}	See figure 4, as applicable	9, 10, 11	01,02, 05,06, 13,14, 22,23, 30,31		50	ns
				42, 43		35	
				03,07, 15,24,32		30	
				04,08, 16,25,33		25	
				09,10, 17,18, 26,27, 34,35		20	
				11,19, 28,36		15	
				47		12	
				12,20, 29,37		10	
				21,38, 41,44, 45,46		7	
				39,40,48		6	
		M,D,P	9 1/	All		2/	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

13

TABLE I. Electrical performance characteristics Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output disable to output in high Z <u>3/ 7/</u>	t _{OHQZ}	See figure 4, as applicable	9, 10, 11	01-08, 13-16, 22-25, 30-33, 42,43		30	ns
				09,10, 17,18, 26,27, 34,35		20	
				11,19, 28,36		15	
				12,20, 29,37		10	
				21,38, 47		8	
				41,44, 45,46		7	
				39,40, 48		6	
				M,D,P	9 <u>1/</u>	All	

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

15

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle time	t _{AVAV}	See figure 4, as applicable	9, 10, 11	01,05, 13,22, 30	120		ns
				02,06, 14,23, 31	100		
				03,07, 15,24, 32	85		
				04,08, 16,25, 33,42, 43	70		
				09,17, 26,34	55		
				10,18, 27,35	45		
				11,19, 28,36	35		
				47	30		
				12,20, 29,37	25		
				21, 38-40	20		
				41,44, 48	15		
				45,46	12		
						M,D,P	
Address setup to beginning of write	t _{AVWL} t _{AVEL}		9, 10, 11	All	0		ns
					<u>2</u> /		
		M,D,P	9 <u>1</u> /				
Data hold after end of write	t _{WHDX} t _{EHDX}		9, 10, 11	01-04	5		ns
				05-48	0		
		M,D,P	9 <u>1</u> /	All	<u>2</u> /		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 16

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write pulse width	t _{WLWH}	See figure 4, as applicable	9, 10, 11	05,13,22,30	100		ns
				06,14,23,31	80		
				07,15, 24,32	70		
				42, 43	65		
				01	50		
				10,18, 27,35 02,03	40		
				04,08, 09,16, 17,25, 26,33, 34	35		
				11,19, 28,36	30		
				12,20, 29,37	20		
				47	22		
				21, 38-40,48	15		
				41,44	12		
				45,46	11		
	M,D,P		9 <u>1/</u>	All	<u>2/</u>		
Address setup to end of write	t _{AVWH}		9, 10, 11	01,05, 13,22, 30	100		ns
Chip select to end of write	t _{ELWH}			02,06, 14,23, 31	85		
				03,07, 15,24, 32	75		
				42, 43	65		
				04,08, 16,25, 33	60		
				09,17, 26,34	45		
				10,18, 27,35	35		
				11,19, 28,36	25		
				47	22		
				12,20, 29,37	20		
				21,38	15		
				39-41,44,48	12		
				45, 46	11		
		M,D,P	9 <u>1/</u>	All	<u>2/</u>		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 17

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address hold after end of write	t _{WHAX} t _{EHAX}	See figure 4, as applicable	9, 10, 11	01-10, 13-18, 22-27, 30-35, 44-46	5		ns
				11, 12, 19-21, 28, 29, 36-43, 47, 48	0		
			M, D, P	9 1/	All	2/	
Data setup to end of write	t _{DVWH} t _{DVEH}	See figure 4, as applicable	9, 10, 11	01, 02, 05, 06, 13, 14, 22, 23, 30, 31	40		ns
				03, 07, 15, 24, 32	35		
				04, 08, 16, 25, 33, 42, 43	30		
				09, 17, 26, 34	25		
				10, 11, 18, 19, 27, 28, 35, 36	20		
				47	18		
				12, 20, 29, 37	15		
				21, 38-40, 48	10		
				41, 44, 45, 46	8		
			M, D, P	9 1/	All	2/	
Write enable to output disable 3/ 7/	t _{WLQZ}	See figure 4, as applicable	9, 10, 11	01-08, 13-16, 22-25, 30-33, 42, 43		35	ns
				09, 10, 17, 18, 26, 27, 34, 35		20	
				11, 19, 28, 36		15	
				12, 20, 29, 37		10	
				21, 38-40, 48		9	
				47		8	
				41, 44-46		7	
			M, D, P	9 1/	All	2/	
Output active after end of write 3/	t _{WHQX}	See figure 4, as applicable	9, 10, 11	All	5		ns
					2/		
			M, D, P	9 1/	All	2/	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 18

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V; 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Retention time <u>3/</u>	t _{CDR}	See figure 4, as applicable	9, 10, 11	All	0		ns
			M,D,P		9 <u>1/</u>	<u>2/</u>	
Operation recovery time <u>3/</u>	t _R		9, 10, 11	01,05, 13,22, 30	120		ns
				02,06, 14,23, 31	100		
				03,07, 15,24, 32	85		
				04,08, 16,25, 33,42, 43	70		
				09,17, 26,34	55		
				10,18, 27,35	45		
				11,19, 28,36	35		
				47	30		
				12,20, 29,37	25		
				21, 38- 40	20		
				41,44, 48	15		
				45,46	12		
		M,D,P	9 <u>1/</u>	All	<u>2/</u>		

1/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ± 5°C. The M, D, and P in the test condition column are the postirradiation limits for the device types specified in the device types column.

2/ Preirradiation values for RHA marked devices shall also be the postirradiation values unless otherwise specified.

3/ This parameter is tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

4/ Functional tests shall include the test table and other test patterns used for fault detection as approved by the qualifying activity. Outputs are measured at V_{OL} < 1.5 V, V_{OH} > 1.5 V.

5/ For timing waveforms see figure 4 and for output load circuits, see figure 5.

6/ AC measurements assume transition time ≤ 5 ns, input levels are from ground to 3.0 V, and output load C_L ≥ 30 pF except as noted on figure 5. Timing reference levels are 1.5 V.

7/ Transition is measured ±500 mV from steady state voltage.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

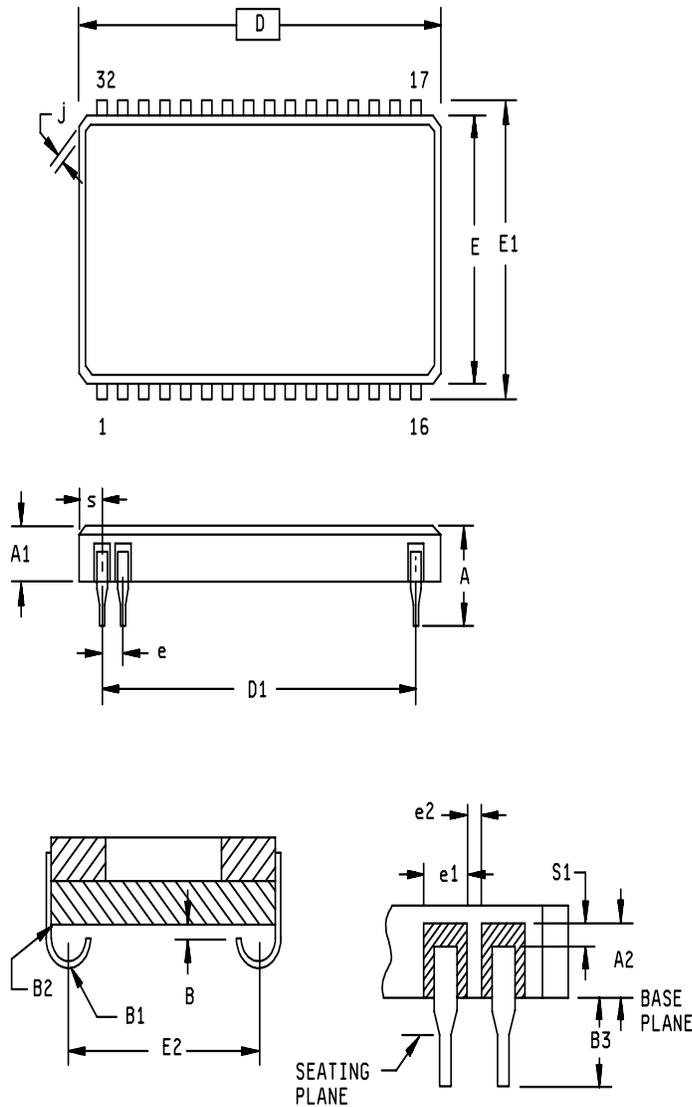
5962-89598

REVISION LEVEL
N

SHEET

19

Case Y



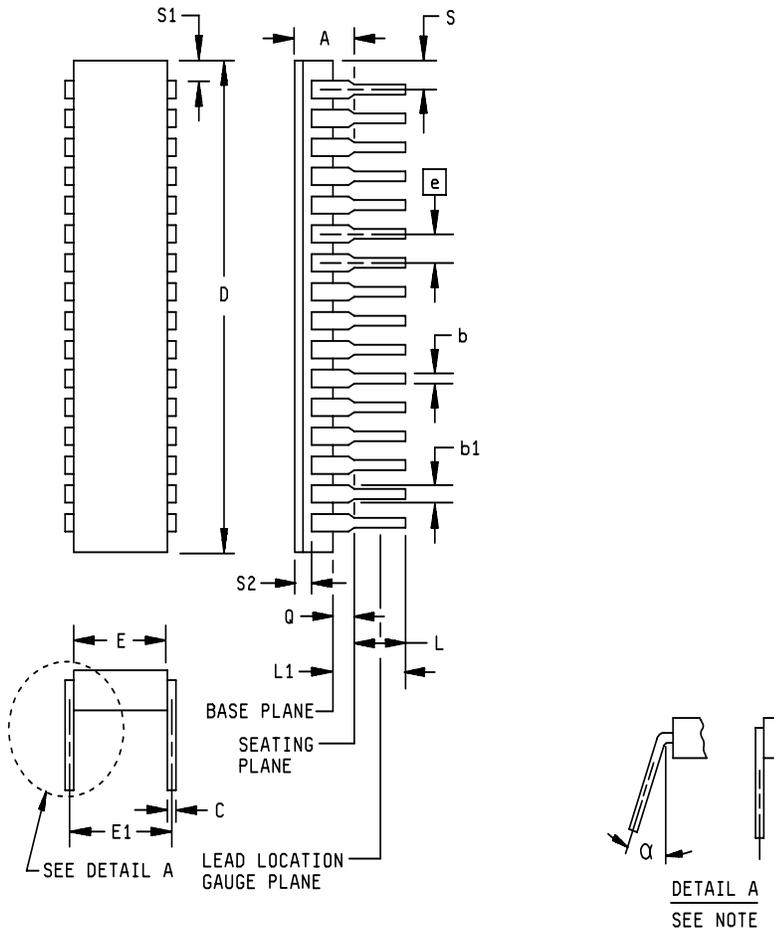
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.120	.165	3.05	4.19
A1	.088	.120	2.24	3.05
A2	.070	Ref.	1.78	---
B	.010	Ref.	0.25	---
B1	.030R	Typ.	0.76	---
B2	.020	Ref.	0.51	---
B3	.025	.045	0.64	1.14
D	.816	.838	20.73	21.29
D1	.750	Ref.	19.05	---
E	.419	.431	10.64	10.95
E1	.430	.445	10.42	11.30
E2	.360	.380	9.14	9.65
e	.050 BSC		1.27 BSC	
e1	.038	Typ.	0.97	---
e2	.005		0.13	---
j	.005	Typ.	0.13	---
S	.030	.040	0.76	1.02
S1	.020	Typ.	0.51	---

NOTE: A bottom brazed package may be shipped as an alternative package style, provided the vendor makes the receiving customer aware of the intent to ship the part as a bottom brazed package rather than the one shown on this figure.

FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 20

Case Z



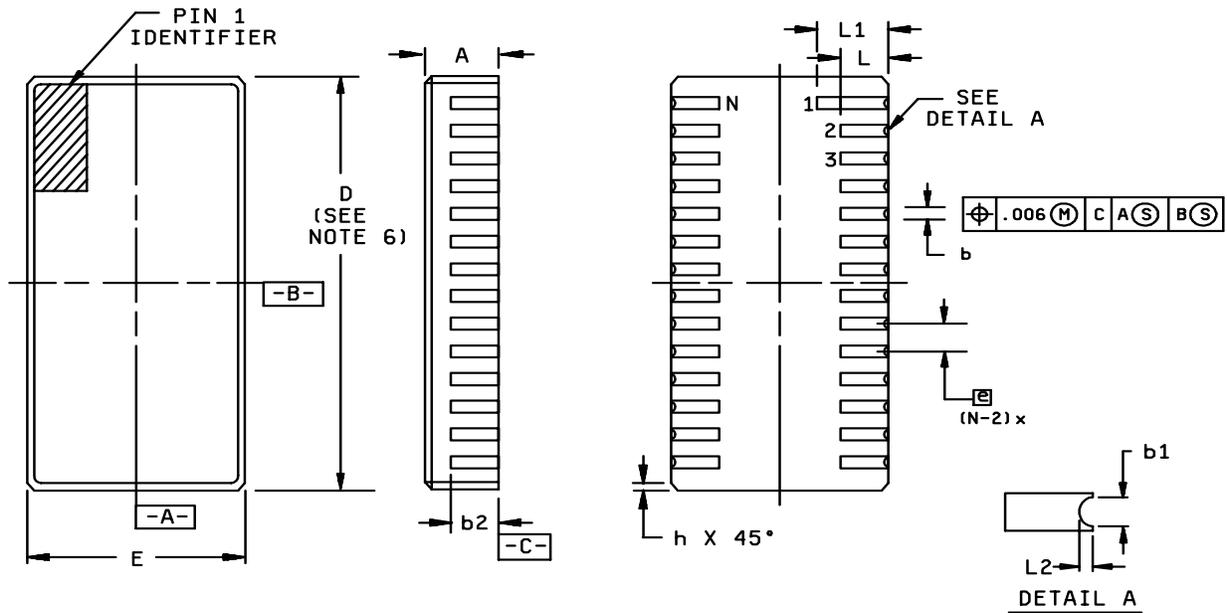
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.232	---	5.89
b	.014	.023	0.36	0.58
b1	.038	.065	0.97	1.65
c	.008	.015	0.20	0.38
D	---	1.700	---	41.05
E	.350	.405	9.78	10.29
E1	.390	.420	9.91	10.67
e	.100 BSC		2.54 BSC	
L	.125	.200	3.18	5.08
L1	.150	---	3.81	---
Q	.015	.060	0.38	1.52
S	---	.100	---	2.54
S1	.005	---	0.13	---
S2	.005	---	0.13	---
α	0°	15°	---	---
N	32			

Note: Either configuration in detail A is allowed.

FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 21

Case U



Symbol	Inches			Millimeters			Notes
	Min	Nom	Max	Min	Nom	Max	
A	.080	.090	.100	2.03	2.29	2.54	
b	.022	.025	.028	0.56	0.64	0.71	
b1	.006	.014	.022	0.15	0.36	0.56	4
b2	.040	---	---	1.02	---	---	
D	.800	.820	.840	20.32	20.83	21.34	
E	.392	.400	.408	9.96	10.16	10.36	
e	.050 BSC			1.27 BSC			
h	.012 REF			0.30 REF			7
L	.070	.075	.080	1.78	1.90	2.03	
L1	.090	.100	.110	2.29	2.54	2.79	5
L2	.003	.009	.015	0.08	0.23	0.38	4
N	32			---			8

FIGURE 1. Case outlines – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 22

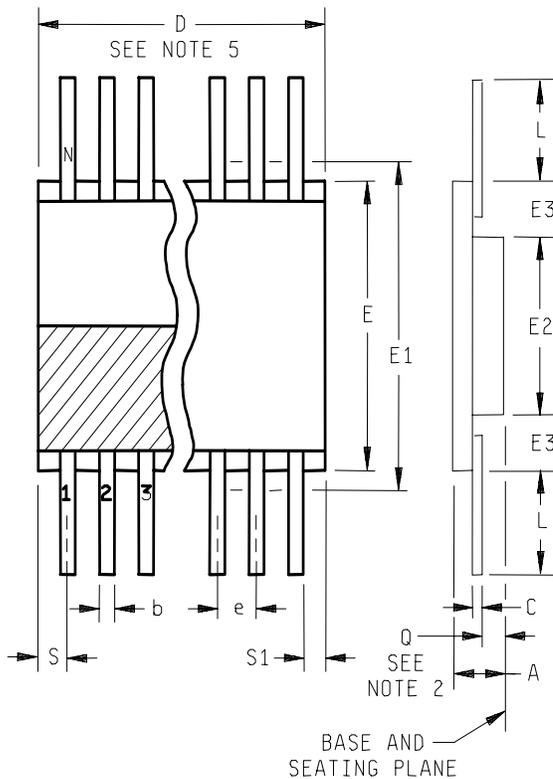
NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. All dimensions and tolerances conform to ANSI Y14.5M-1982.
4. Metallized castellations shall be connected to plane 1 terminals.
5. Index area: A pin identification mark shall be located adjacent to pin one within the shaded area shown. Plane 1 terminal identification may be an extension of the length of the metallized terminal which shall not be wider than the b dimension.
6. The cover shall not extend beyond the edges of the body.
7. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option.
8. N indicates the number of terminals.
9. Unless otherwise specified, a minimum clearance of .015 inch (.381 mm) shall be maintained between all metallized features (e.g., lid, castellation, terminals, thermal pads, etc.).
10. Solder finish is optional with a maximum allowable thickness of .007 inch. Measurement of dimensions A, b1, and L2 may be made prior to solder application.

FIGURE 1. Case outlines – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 23

Case T



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.097	.125	2.46	3.18	
b	.015	.019	0.38	0.48	5
c	.003	.009	0.08	0.23	5
D	---	.830	---	21.08	3
E	.400	.420	10.16	10.67	
E1	---	.450	---	11.43	3
E2	.180	---	4.57	---	
E3	.030	---	0.76	---	9
e	.050 BSC		1.27 BSC		4,6
L	.250	.370	6.35	9.40	
Q	.020	.045	0.51	1.14	
S	---	.045	---	1.14	7
S1	.000	---	0.00	---	7,8
N	32				6

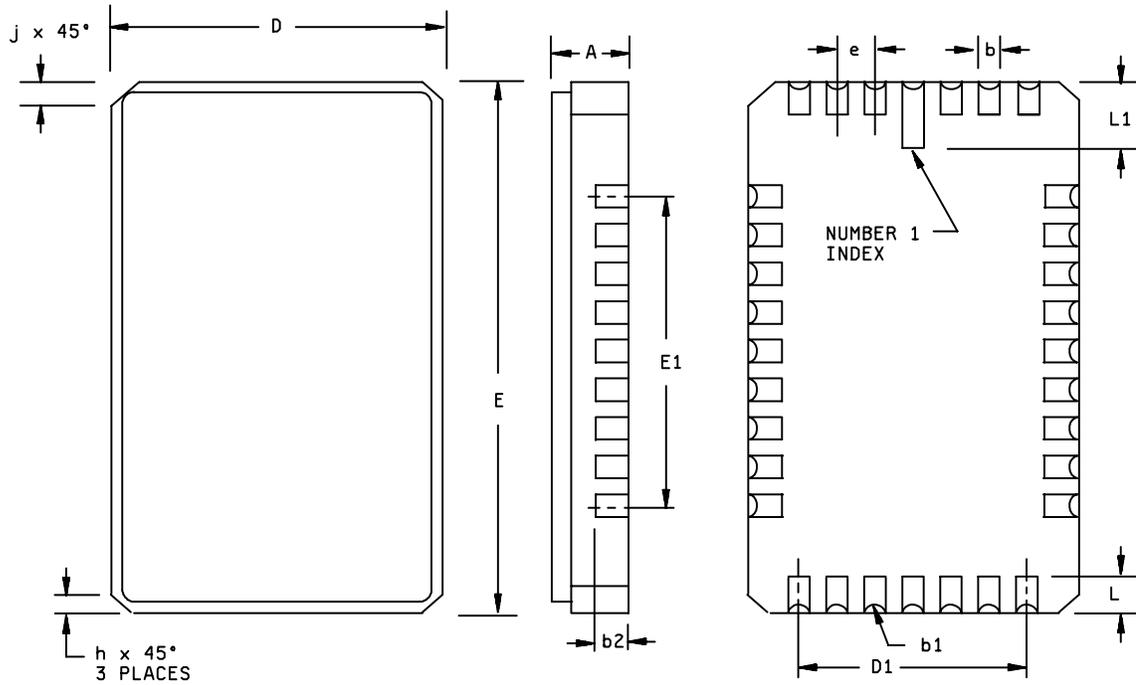
NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body. Dimension Q minimum shall be reduced by .0015 inch (0.038 mm) maximum when lead finish A is applied.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic lead spacing is .050 (1.27 mm) between centerlines. Each lead centerline shall be located within ± 0.005 (0.13 mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.
5. All leads - Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
6. Total number of spaces = (N-2). Symbol "N" is the maximum number of leads.
7. Measure all four corner leads.
8. Dimension S1 (see 5.2.2 of MIL-STD-1835) may be .000 (0.00 mm) if the corner leads, upon entering the body of the package, and within one lead's width, bend toward the die cavity. See 5.2.2 of MIL-STD-1835 for measurement of S1 on bottom-brazed flat packs.
9. Bottom brazed lead configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Dimensions are in inches.
11. Metric equivalents are given for general information only.

FIGURE 1. Case outlines – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 24

Case N



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.070	.100	1.78	2.54
b	.022	.028	0.56	0.71
b1	.009 R		.23 R	
b2	.038	.042	.97	1.07
D	.445	.460	11.30	11.68
D1	.295	.305	7.49	7.75
E	.695	.715	17.65	---
E1	.395	.405	10.03	10.29
e	.050 TYP		1.27 TYP	
h	.020 REF		.51 REF	
J	.035 REF		.89 REF	
L	.045	.055	1.14	1.40
L1	.077	.093	1.96	2.36

FIGURE 1. Case outlines – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 25

Case 9

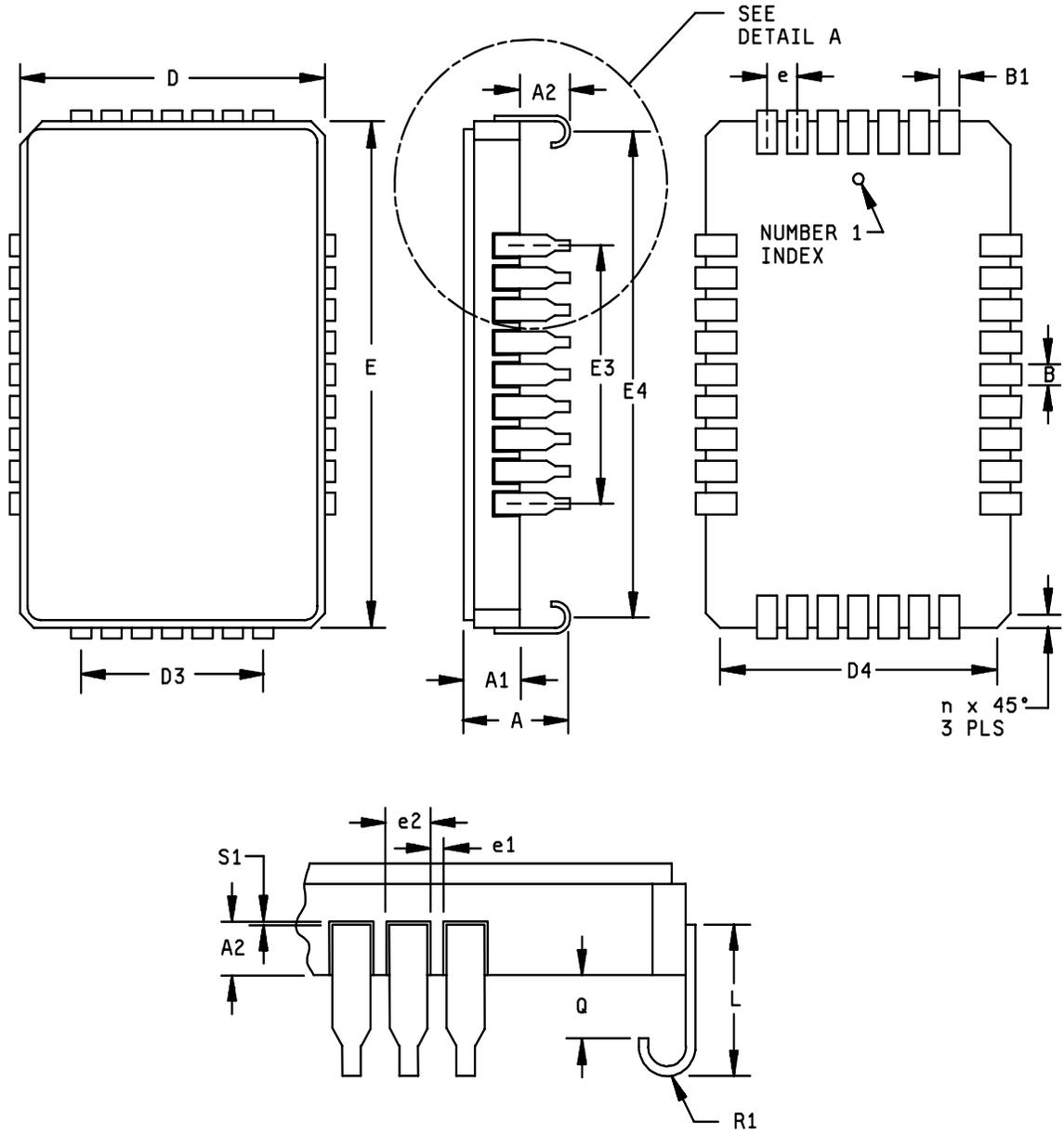


FIGURE 1. Case outlines – Continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

26

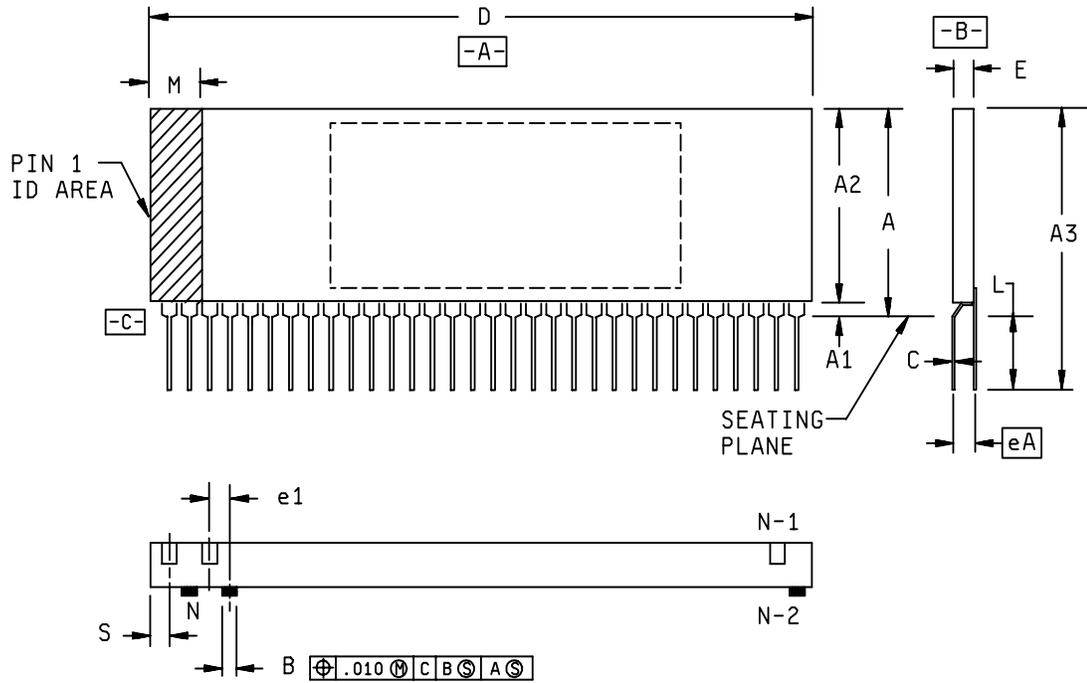
Case 9 – Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.141	.177	3.58	4.50
A1	.073	.089	1.85	2.26
A2	.078 REF		1.98 REF	
A3	.033	.065	.84	1.65
B	.017 REF		.43 REF	
B1	.028 REF		.71 REF	
D	.445	.458	11.30	11.63
D3	.290	.310	7.37	7.87
D4	.400	.440	10.16	11.18
E	.695	.710	17.65	18.03
E3	.390	.410	9.91	10.41
E4	.650	.690	16.51	17.53
e	.050 TYP		1.27 TYP	
e1	.007 REF		.18 REF	
h	.020 REF		.51 REF	
L	.075	.115	1.91	2.92
Q	.040 MIN		1.02 MIN	
R1	.023 R REF TYP		.58 R REF TYP	
S1	.003	.035	.08	.89

FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 27

Case 8



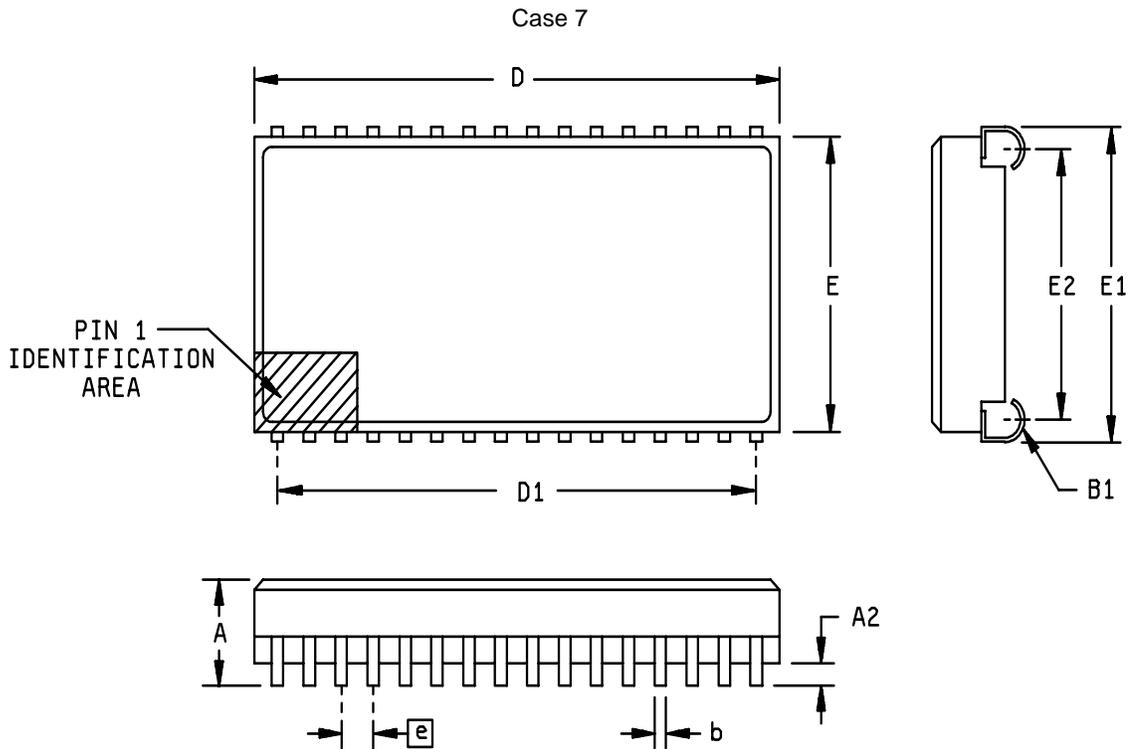
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.460	.500	11.68	12.70	3
A1	.020	.040	0.51	1.02	
A2	.440	.460	11.18	11.68	
A3	.565	.645	14.35	16.38	
B	.016	.020	0.41	0.51	
C	.008	.012	0.20	0.30	
D	1.630	1.670	41.40	42.42	6
E	.090	.130	2.29	3.30	
e1	.050 BSC		1.27 BSC		
eA	.100 BSC		2.54 BSC		
L	.125	.155	3.18	3.95	
M	.055	.105	1.40	2.67	
N	32				1
S	.030	.070	0.76	1.78	

NOTES:

1. N is the number of leads.
2. The chamfer on the body is optional. If is not present, a visual index feature must be located within the cross hatched area.
3. Lead configuration in this area is optional.
4. Controlling dimension: Inches.
5. Solder finish is optional. However, if leads are solder dipped or plated, increase maximum limit of all leads by 0.003" from center of flat.
6. The cover shall not extend beyond the edges of the ceramic body.

FIGURE 1. Case outlines - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 28



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.35	3.66	.132	.144
A2	0.66	0.91	.026	.036
b	0.38	0.48	.015	.019
B1	0.76	1.02	.030	.040
D	20.62	21.03	.812	.828
D1	18.80	19.30	.740	.760
E	10.29	10.54	.405	.415
E1	11.05	11.30	.435	.445
E2	9.14	9.85	.360	.380
e	1.27 BSC		.050 BSC	
N	32			

FIGURE 1. Case outlines - continued.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-89598

REVISION LEVEL
N

SHEET

29

Device types	01 through 12, 22 through 29,39, 40,42 through 46	13 through 21, 30 through 38, 41,47	01 through 12, 22 through 29, 39
Case outlines	X, Y, Z, U, T, N, M, 9, and 7		8
Terminal number	Terminal symbol		
1	NC	NC	NC
2	A ₁₆	A ₁₆	V _{CC}
3	A ₁₄	A ₁₄	A ₁₆
4	A ₁₂	A ₁₂	A ₁₅
5	A ₇	A ₇	A ₁₄
6	A ₆	A ₆	NC
7	A ₅	A ₅	A ₁₂
8	A ₄	A ₄	\overline{WE}
9	A ₃	A ₃	A ₇
10	A ₂	A ₂	A ₁₃
11	A ₁	A ₁	A ₆
12	A ₀	A ₀	A ₈
13	I/O ₀	I/O ₀	A ₅
14	I/O ₁	I/O ₁	A ₉
15	I/O ₂	I/O ₂	A ₄
16	V _{SS}	V _{SS}	A ₁₁
17	I/O ₃	I/O ₃	A ₃
18	I/O ₄	I/O ₄	\overline{OE}
19	I/O ₅	I/O ₅	A ₂
20	I/O ₆	I/O ₆	A ₁₀
21	I/O ₇	I/O ₇	A ₁
22	\overline{CE}	\overline{CE}_1	\overline{CS}
23	A ₁₀	A ₁₀	A ₀
24	\overline{OE}	\overline{OE}	I/O ₇
25	A ₁₁	A ₁₁	I/O ₀
26	A ₉	A ₉	I/O ₆
27	A ₈	A ₈	I/O ₁
28	A ₁₃	A ₁₃	I/O ₅
29	\overline{WE}	\overline{WE}	I/O ₂
30	NC	CE ₂	I/O ₄
31	A ₁₅	A ₁₅	V _{SS}
32	V _{CC}	V _{CC}	I/O ₃

NC = No connection

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 30

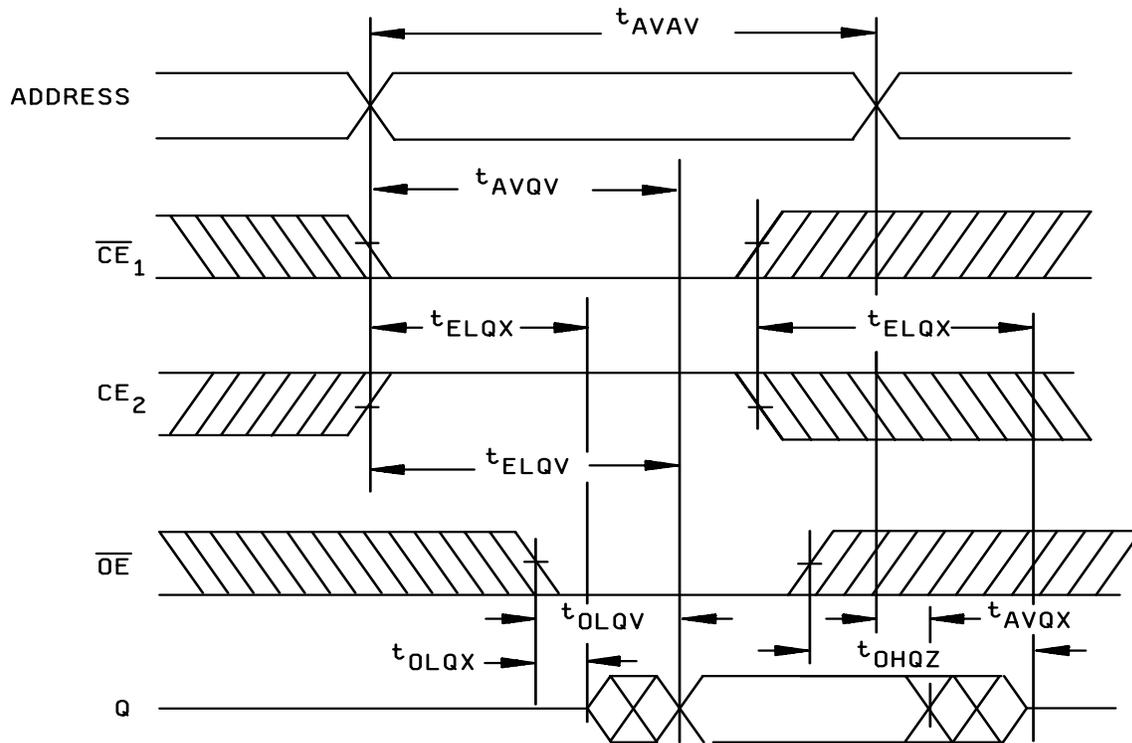
Mode	\overline{CE}	*CE ₂	\overline{WE}	\overline{OE}	I/O
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Read	L	H	H	L	D _{OUT}
Write	L	H	L	X	D _{IN}
Read	L	H	H	H	High Z

H = logic "1" state, L = logic "0" state.
X = logic "don't care" state, and Z = high impedance state.
* = only applies to devices with dual \overline{CE} .

FIGURE 3. Truth table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 31

Read Cycle (see notes 1 and 2)



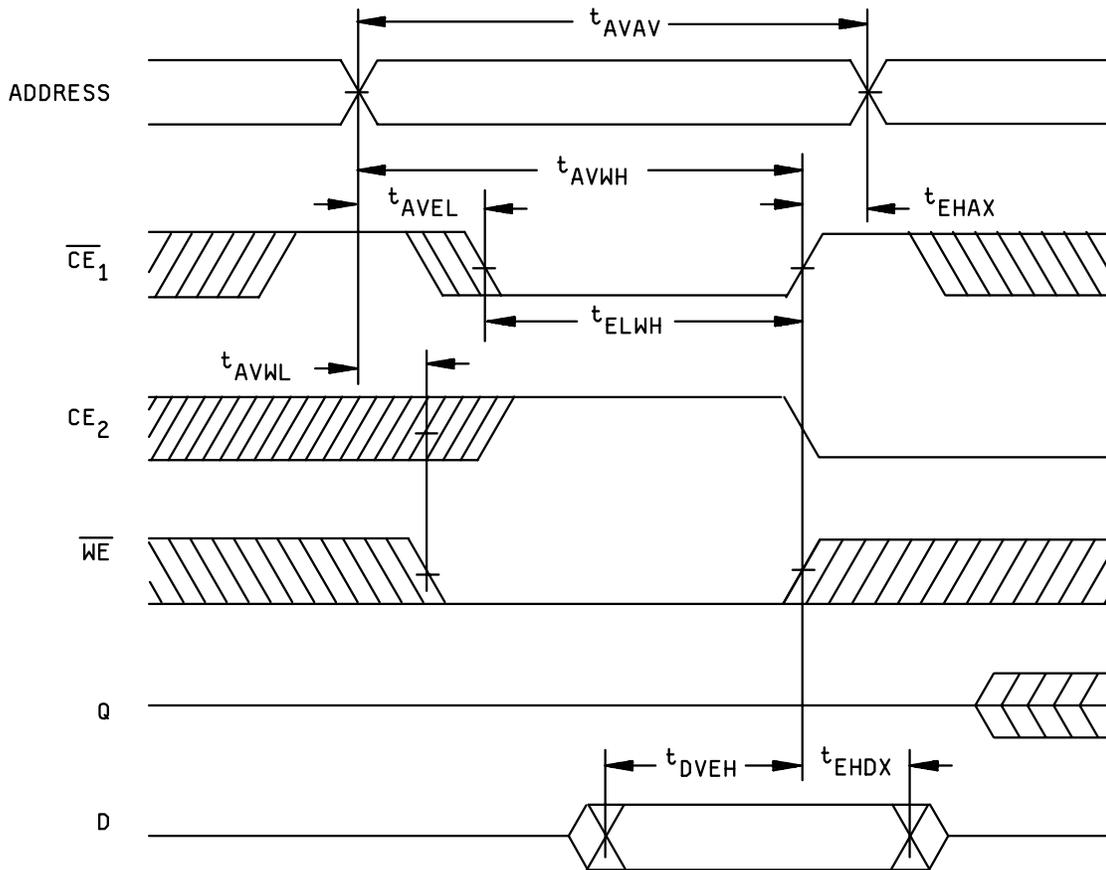
NOTES:

1. \overline{WE} is held high during the read cycle.
2. Timing measurement reference level is 1.5 V.

FIGURE 4. Timing waveform diagrams.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 32

Write cycle 1 (see notes 1, 2, and 3)
(\overline{CE}_1 or CE_2 controlled)



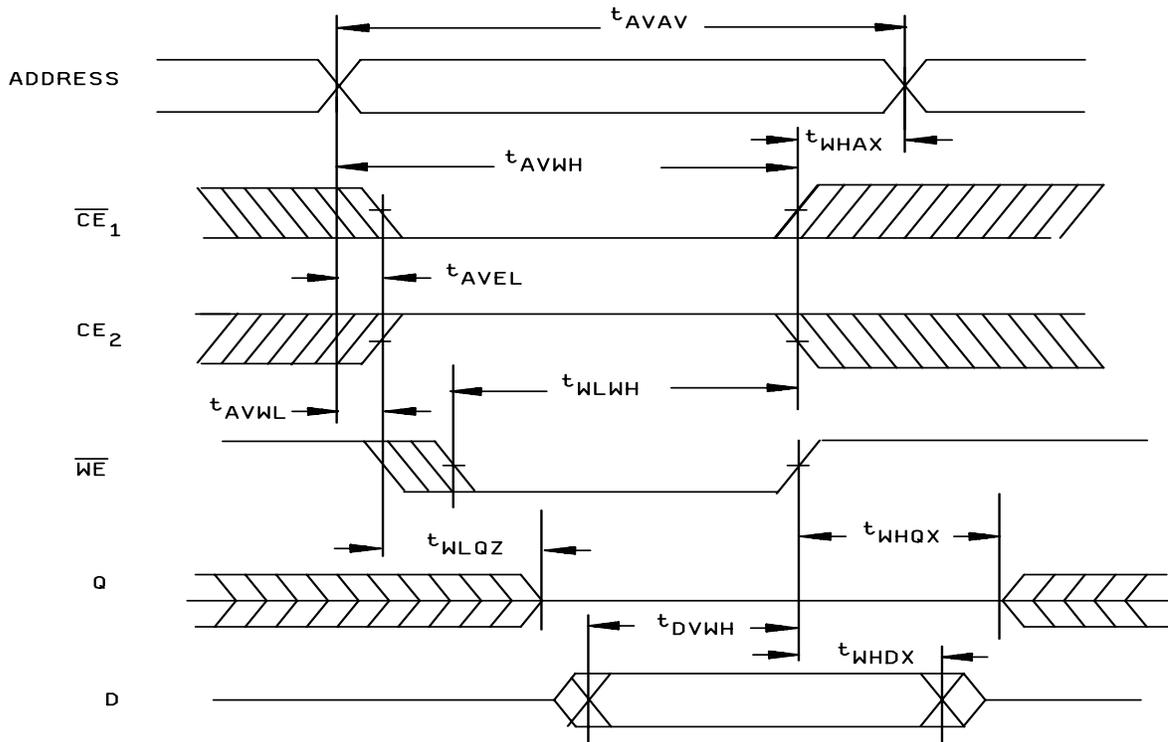
NOTES:

1. Either \overline{CE}_1 or CE_2 may be used to control the write cycle. If \overline{CE}_1 is used, CE_2 should be high when \overline{WE} is low. If CE_2 is used, \overline{CE}_1 should be low when \overline{WE} is low.
2. In a \overline{CE}_1 or CE_2 controlled write cycle, the outputs assume a high impedance state, whether \overline{OE} is high or low, as long as \overline{WE} is low.
3. Timing measurement reference is 1.5 V.

FIGURE 4. Timing waveform diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 33

Write cycle 2 (see notes 1 and 2)
 (\overline{WE} controlled)



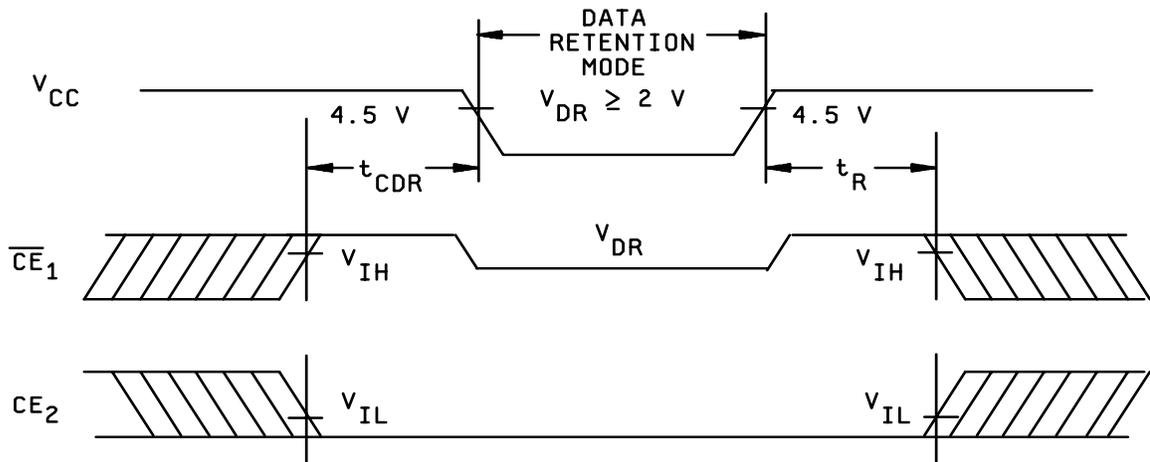
NOTES:

1. In the \overline{WE} controlled write cycle, while \overline{WE} is low, it will force the outputs into a high impedance state, whether \overline{OE} is high or low.
2. Timing measurement reference level is 1.5 V.

FIGURE 4. Timing waveform diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 34

Data retention Waveform (see notes 1 and 2)

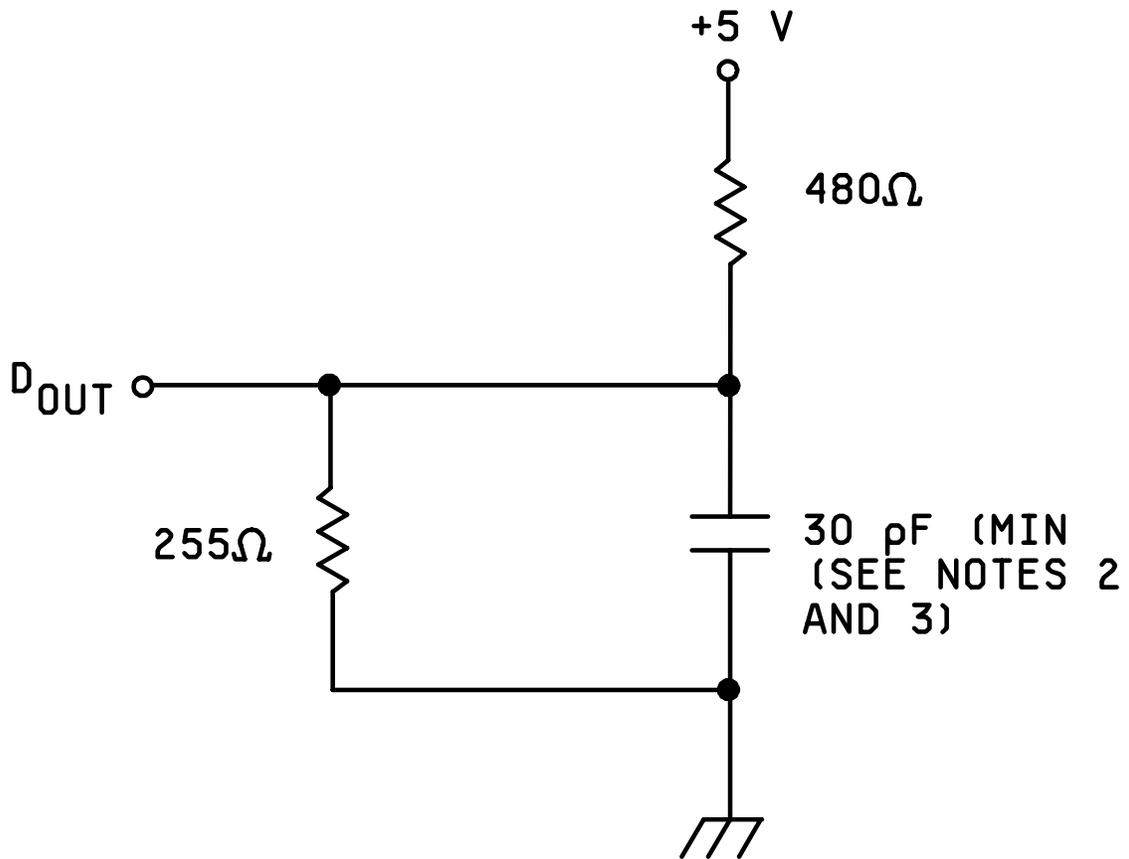


NOTES:

1. Either \overline{CE}_1 or CE_2 may be used to begin data retention mode.
2. For t_{CDR} and t_R : $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IH} \geq V_{CC} - 2.0V$ or $V_{IH} \leq 0.2V$.

FIGURE 4. Timing waveform diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 35

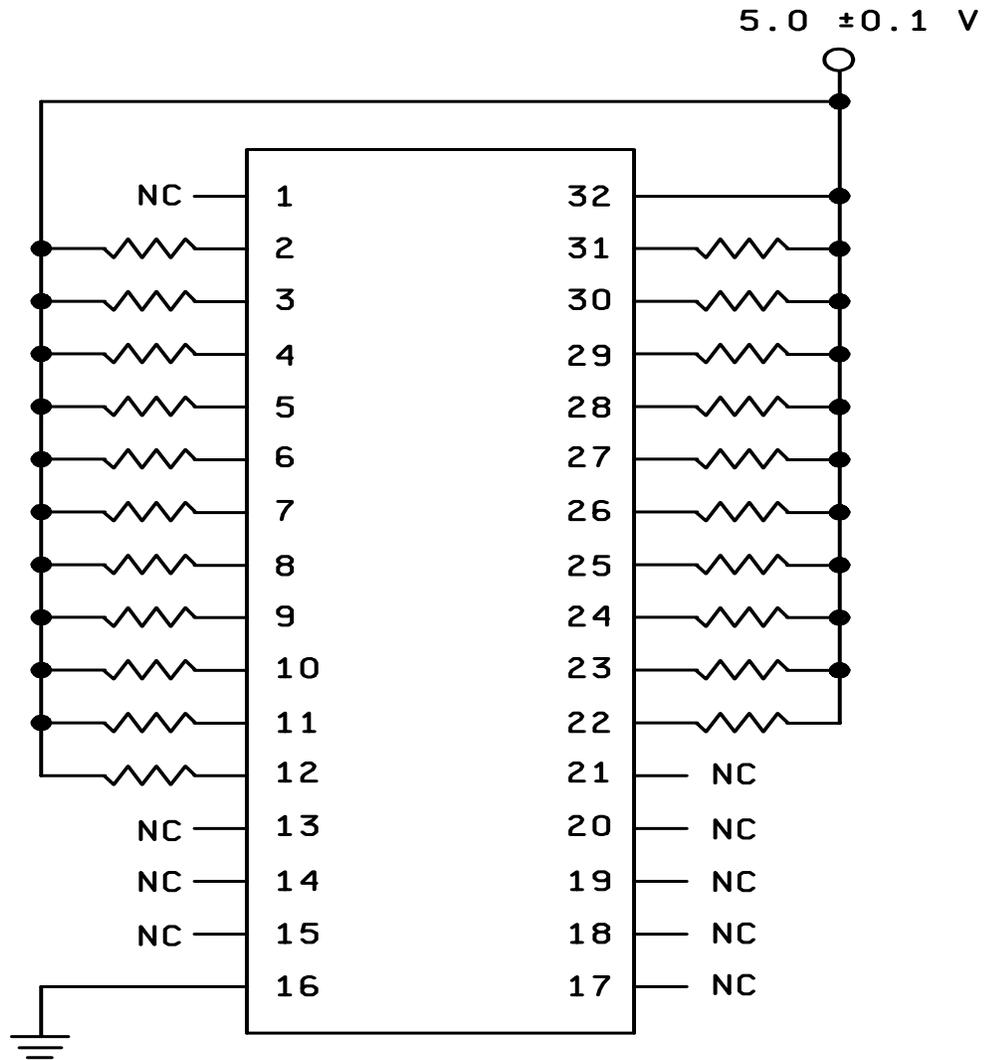


NOTES:

1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{EHQZ} , t_{OHQZ} , t_{ELQX} , t_{OLQX} , and t_{WHQX} .

FIGURE 5. Output load circuits.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 36



NOTE: Input protection resistors = 1 kΩ.

FIGURE 6. Bias conditions for irradiation testing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 37

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I _{CC3} standby	±10% of specified value in table I
I _{IH} , I _{IL}	±10% of specified value in table I
I _{OHZ} , I _{OLZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 38

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. T_A = +125°C, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 39

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup shall not occur under any recommended operating condition.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

- a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.
- b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.
- c. The transient dose rate upset level shall be greater than or equal to 5^{10} rads(Si)/s with a pulse width less than or equal to 1.0 μs .

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^{\circ} \leq \text{angle} \leq 60^{\circ}$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The test temperature shall be $+25^{\circ}\text{C}$ and the maximum rated operating temperature $\pm 10^{\circ}\text{C}$.
- f. Bias conditions shall be $V_{CC} = 4.5$ V dc for the upset measurements and $V_{CC} = 5.5$ V dc for the latchup measurements.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 40

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

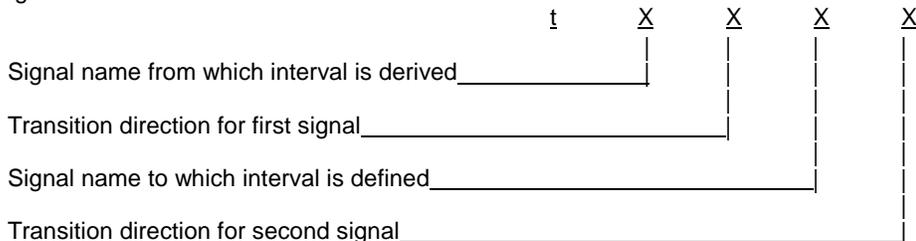
6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

- C_{IN}, C_{OUT} Input and bi-directional output, terminal-to-GND capacitance.
- GND Ground zero voltage potential.
- I_{CC} Supply current.
- I_{IL} Input current low.
- I_{IH} Input current high.
- T_C Case temperature.
- T_A Ambient temperature.
- V_{CC} Positive supply voltage.
- V_{IC} Positive input clamp voltage.
- O/V Latch-up over-voltage.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transitions. Thus the format is:



STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 41

6.5.1 Timing parameter abbreviations – Continued.

a. Signal definitions:

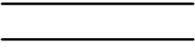
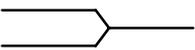
- A = Address
- D = Data in
- Q = Data out
- W = Write enable
- E = Chip enable
- O = Output enable

b. Transition definitions:

- H = Transition to high
- L = Transition to low
- V = Transition to valid
- X = Transition to invalid or don't care
- Z = Transition to off (high impedance)

6.5.2.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 42

APPENDIX A
FORMS A PART OF SMD 5962-89598

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 43

APPENDIX A - Continued.

30.3 Algorithm C (pattern 3).

30.2.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 44

APPENDIX B
FORMS A PART OF SMD 5962-89598

SUBSTITUTION DATA

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. For new designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows:

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. SUBSTITUTION DATA

<u>NEW PIN</u>	<u>OLD PIN</u>
5962-8959801MXX	5962-8959801XX
5962-8959802MXX	5962-8959802XX
5962-8959803MXX	5962-8959803XX
5962-8959804MXX	5962-8959804XX

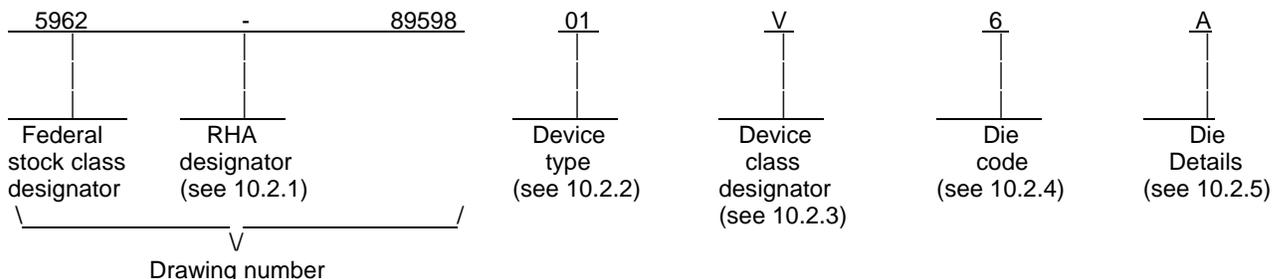
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	REVISION LEVEL N	5962-89598 SHEET 45
---	------------------	---------------------	--------------------------------------

APPENDIX C
FORMS A PART OF SMD 5962-89598

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
47	65608EV-30	128K X 8 very low power CMOS SRAM	30ns

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 6 for all devices supplied as die only with no case outline.

10.2.5 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 46

APPENDIX C
FORMS A PART OF SMD 5962-89598

10.2.5.1 Die physical dimensions.

Die type	Figure number
01	A-1

10.2.5.2. Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

10.2.5.3. Interface materials.

Die type	Figure number
01	A-1

10.2.5.4. Assembly related information.

Die type	Figure number
01	A-1

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 47

APPENDIX C
FORMS A PART OF SMD 5962-89598

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3. of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4. of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The manufacturer's modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

- a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.
- b) 100% wafer probe (see paragraph 30.4).
- c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-89598
	REVISION LEVEL N	SHEET 48

APPENDIX C
FORMS A PART OF SMD 5962-89598

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1., 4.4.4.2, 4.4.4.3 and 4.4.4.4.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 49

APPENDIX C
FORMS A PART OF SMD 5962-89598

Pad number Top left corner	Pad reference	Position relative to center of die (dimensions are in millimeters)		Rotation angle In degrees	Manufacturer Pad reference	Signal name
		X	Y			
1	A	-7,706	2,297	0	20	(A3)
2	A	-7,706	2,117	0	21	(A2)
3	A	-7,706	1,937	0	22	(A1)
4	A	-7,706	1,757	0	23	(A0)
5	A	-7,706	1,522	0	24	(1/O0)
6	A	-7,706	1,242	0	25	I/O1
7	A	-7,706	0,992	0	26	Gnd
8	A	-7,706	0,742	0	27	I/O2
9	A	-7,706	0,242	0	28	Gnd
10	B	-7,706	0,042	0	29	Gnd
11	A	-7,706	-0,158	0	30	Gnd
12	A	-7,706	-0,408	0	31	I/O3
13	A	-7,706	-0,688	0	32	I/O4
14	A	-7,706	-0,913	0	33	Gnd
15	A	-7,706	-1,138	0	34	I/O5
16	A	-7,706	-1,418	0	35	(I/O6)
17	A	-7,706	-1,698	0	36	(I/O7)
18	A	-7,706	-1,938	0	37	(CS1/)
19	A	-7,706	-2,118	0	38	(A10)
20	A	-7,706	-2,298	0	39	(OE/)
21	A	-7,488	-2,504	0	40	I/O6
22	A	-7,227	-2,504	0	41	Gnd
23	A	-6,947	-2,504	0	42	I/O7
24	A	-5,787	-2,504	0	43	CS1/
25	A	-4,787	-2,504	0	44	A10
26	A	-3,787	-2,504	0	45	OE/
27	A	-0,187	-2,504	0	46	Gnd
28	A	3,813	-2,504	0	47	All
29	A	4,813	-2,504	0	48	A9

Figure A-1, MMO-65608EV Bond Pad Locations and Functions

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 50

APPENDIX C
FORMS A PART OF SMD 5962-89598

Pad number Top left corner	Pad reference	Position relative to center of die (dimensions are in millimeters)		Rotation angle In degrees	Manufacturer Pad reference	Signal name
		X	Y			
30	A	5,813	-2,504	0	49	A8
31	A	6,613	-2,504	0	50	A13
32	A	7,213	-2,504	0	51	W/
33	A	7,729	-2,333	0	52	(A11)
34	A	7,729	-2,158	0	53	(A9)
35	A	7,729	-1,983	0	54	(A8)
36	A	7,729	-1,808	0	55	(A13)
37	A	7,729	-1,633	0	56	(W)
38	A	7,729	-1,407	0	57	CS2
39	A	7,729	-1,183	0	58	Gnd
40	A	7,729	-0,983	0	59	A15
41	A	7,729	-0,188	0	60	Vcc
42	B	7,722	0,042	0	61	Vcc
43	A	7,729	0,272	0	62	Vcc
44	A	7,729	0,842	0	1	A16
45	A	7,729	1,067	0	2	Gnd
46	A	7,729	1,267	0	3	A14
47	A	7,729	1,436	0	4	(A12)
48	A	7,729	1,617	0	5	(A7)
49	A	7,729	1,792	0	6	(A6)
50	A	7,729	1,967	0	7	(A5)
51	A	7,729	2,142	0	8	(A4)
52	A	7,729	2,323	0	9	A12
53	A	7,638	2,504	0	10	A7
54	A	6,813	2,504	0	11	A6
55	A	6,613	2,504	0	12	A5
56	A	4,413	2,504	0	13	A4
57	A	0,013	2,504	0	14	Gnd
58	A	-3,787	2,804	0	15	A3
59	A	-4,787	2,504	0	16	A2
60	A	-6,787	2,504	0	17	A1
61	A	-6,387	2,504	0	18	A0
62	A	-7,481	2,504	0	19	I/O0

Figure A-1, MMO-65608EV Bond Pad Locations and Functions – Continued

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-89598
		REVISION LEVEL N	SHEET 51

APPENDIX C
FORMS A PART OF SMD 5962-89598

□19	□18	□17	□16	□15	□14	□13	□12	□11	□10	9□	8□	7□	6□	5□	4□	3□	2□	1□	62□	61□	60□	59□	58□	57□	56□	55□	54□	53□	52□		
□20	□21	□22	□23	□24	□25	□26	□27	□28	□29	□30	□31	□32	□33	□34	□35	□36	□37	□38	□39	□40	41□	42□	43□	44□	45□	46□	47□	48□	49□	50□	51□

Die physical dimensions.

Die size: 15 860 X 5 410 microns
Die thickness: 475 microns

Interface materials.

Top metallization: Aluminium + 1% Copper
Backside metallization: bare silicon

Glassivation.

Type: Silicon Oxide + Nitride
Thickness: 15 000 Angstroms

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: not connected
Special assembly instructions: None

Figure A-1, MMO-65608EV Bond Pad Locations and Functions – Continued

<p>STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</p>	<p>SIZE A</p>		<p>5962-89598</p>
		<p>REVISION LEVEL N</p>	<p>SHEET 52</p>