

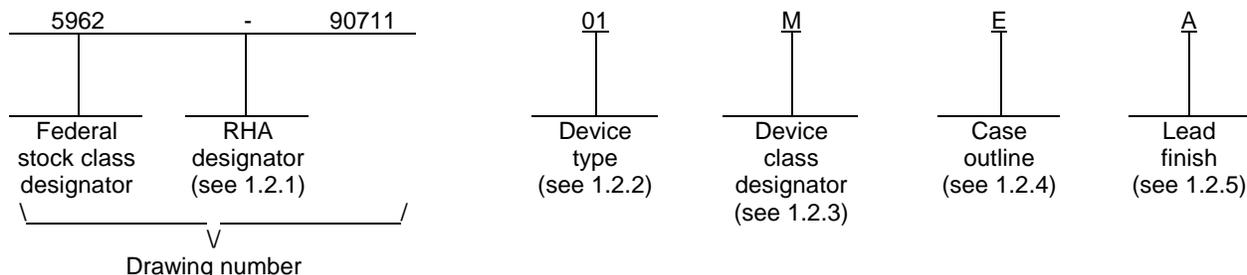
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. -rrp	04-06-29	R. MONNIN

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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY DAN WONNELL				<b>DEFENSE SUPPLY CENTER COLUMBUS</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.dsc.dla.mil">http://www.dsc.dla.mil</a>															
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS  AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY CHARLES E. BESORE																			
	APPROVED BY MICHAEL A. FRYE				<b>MICROCIRCUIT, LINEAR, MICROPROCESSOR SUPERVISORY CIRCUITS, MONOLITHIC SILICON</b>															
	DRAWING APPROVAL DATE 92-03-26																			
	REVISION LEVEL A				SIZE A	CAGE CODE <b>67268</b>	<b>5962-90711</b>													
				SHEET 1 OF 13																

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	MAX691	Microprocessor watchdog/battery switchover/reset generator
02	MAX693	Microprocessor watchdog/battery switchover/reset generator
03	MAX695	Microprocessor watchdog/battery switchover/reset generator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ).....	-0.3 V dc to +6.0 V dc
Battery voltage range ( $V_{BATT}$ ).....	-0.3 V dc to +6.0 V dc
All other inputs .....	-0.3 V dc to ( $V_{OUT} + 0.5$ V)
Input current:	
$V_{CC}$ .....	+200 mA
$V_{BATT}$ .....	+50 mA
GND .....	+20 mA
Output current:	
$V_{OUT}$ .....	Short circuit protected
All other outputs .....	+20 mA
Rate-of-rise, $V_{BATT}$ , $V_{CC}$ .....	+100 V/ $\mu$ s
Storage temperature range .....	-65°C to +160°C
Lead temperature (soldering, 4 seconds).....	260°C
Power dissipation ( $P_D$ ) .....	600 mW 2/
Lead temperature (soldering, 10 seconds) .....	300°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	+50°C/W
Thermal resistance, junction-to-ambient ( $\theta_{JA}$ ) .....	+100°C/W

1.4 Recommended operating conditions.

Supply voltage ( $V_{CC}$ ):	
Device types 01 and 03 .....	4.75 V dc to 5.5 V dc
Device type 02 .....	4.5 V dc to 5.5 V dc
Battery voltage ( $V_{BATT}$ ).....	2.8 V
Ambient operating temperature range ( $T_A$ ).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or [www.dodssp.daps.mil](http://www.dodssp.daps.mil) or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
 2/ Derate 10 mW/°C above +85°C.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>BATT</sub> = 2.8 V unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit	
					Min	Max		
<b>BATTERY BACKUP SWITCHING</b>								
Operating voltage range	V <sub>CC</sub>		1, 2, 3	01, 03	4.75	5.5	V	
				02	4.5	5.5		
	V <sub>BATT</sub>			01, 03	2.0	4.25		
				02	2.0	4.0		
Output voltage	V <sub>OUT</sub>	I <sub>OUT</sub> = 1 mA	1, 2, 3	All	V <sub>CC</sub> -0.3		V	
		I <sub>OUT</sub> = 50 mA			V <sub>CC</sub> -0.5			
Battery output voltage backup mode	BATT <sub>OUT</sub>	I <sub>OUT</sub> = 250 μA, V <sub>CC</sub> < V <sub>BATT</sub> -0.2 V	1, 2, 3	All	V <sub>BATT</sub> -0.1		V	
Supply current (excluding I <sub>OUT</sub> )	I <sub>CC</sub>	I <sub>OUT</sub> = 1 mA	1	All		5	mA	
			2, 3			7		
		I <sub>OUT</sub> = 50 mA	1			10		
			2, 3			15		
Supply current in battery backup mode	I <sub>BATT</sub>	V <sub>CC</sub> = V, V <sub>BATT</sub> = 2.8 V	1	All		1	μA	
			2, 3			10		
Battery standby current (- = charge + = discharge)	I <sub>BATT</sub> SB	5.5 V > V <sub>CC</sub> > V <sub>BATT</sub> + 1 V	1	All		-0.1	+0.02	μA
			2, 3			-1.0	+0.02	
Battery switchover threshold V <sub>CC</sub> - V <sub>BATT</sub>	BATT <sub>SWTH</sub>	Power up or power down	1, 2, 3	All	-200	+200	mV	
BATT ON output voltage	BATT ON <sub>OUT</sub>	I <sub>SINK</sub> = 3.2 mA	1, 2, 3	All		0.4	V	
BATT ON output short circuit current	BATT ON <sub>IOS</sub>	BATT ON = V <sub>OUT</sub>	1, 2, 3	All		60	mA	
		BATT ON = 0 V				0.1		25
<b>RESET AND WATCHDOG TIMING</b>								
Reset voltage threshold	R <sub>TH</sub>		1, 2, 3	01, 03	4.5	4.75	V	
				02	4.25	4.5		
Reset threshold hysteresis	R <sub>THH</sub>		1, 2, 3	All		250	mV	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>BATT</sub> = 2.8 V unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
RESET AND WATCHDOG TIMING – continued							
Reset timeout delay	R <sub>DEL</sub>	OSC SEL HIGH V <sub>CC</sub> = 5 V	9	01, 02	35	70	ms
			10, 11		31	78	
			9	03	140	280	
			10, 11		126	310	
Watchdog timeout period, internal oscillator	WD <sub>INT</sub>	Long period, V <sub>CC</sub> = 5 V	9	All	1.0	2.25	s
			10, 11		0.9	2.42	
		Short period, V <sub>CC</sub> = 5 V	9		70	140	ms
			10, 11		62	154	
Watchdog timeout period external clock	WD <sub>EXT</sub>	Long period	9, 10, 11	All	3840	4097	Clock cycles
		Short period			768	1025	
Minimum WDI input pulse width	WDI <sub>PW</sub>	V <sub>IL</sub> = 0.4 V, V <sub>IH</sub> = V <sub>CC</sub> (0.8)	9	All	200		ns
			10, 11		300		
$\overline{\text{RESET}}$ output voltage high	$\overline{\text{R}}_{\text{VOH}}$	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V	1, 2, 3	All	3.5		V
$\overline{\text{RESET}}$ output voltage low	$\overline{\text{R}}_{\text{VOL}}$	I <sub>SINK</sub> = 1.6 mA, V <sub>CC</sub> = 4.25 V	1	All		0.4	V
		I <sub>SINK</sub> = 800 μA, V <sub>CC</sub> = 4.25 V	2, 3			0.4	
$\overline{\text{LOW LINE}}$ output voltage high	$\overline{\text{LL}}_{\text{VOH}}$	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V	1, 2, 3	All	3.5		V
$\overline{\text{LOW LINE}}$ output voltage low	$\overline{\text{LL}}_{\text{VOL}}$	I <sub>SINK</sub> = 1.6 mA, V <sub>CC</sub> = 4.25 V	1	All		0.4	V
		I <sub>SINK</sub> = 800 μA, V <sub>CC</sub> = 4.25 V	2, 3			0.4	
$\overline{\text{WDO}}$ output voltage high	$\overline{\text{WDO}}_{\text{VOH}}$	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V	1, 2, 3	All	3.5		V
$\overline{\text{WDO}}$ output voltage low	$\overline{\text{WDO}}_{\text{VOL}}$	I <sub>SINK</sub> = 1.6 mA, V <sub>CC</sub> = 4.25 V	1	All		0.4	V
		I <sub>SINK</sub> = 800 μA, V <sub>CC</sub> = 4.25 V	2, 3			0.4	
RESET output voltage high	RESET <sub>VOH</sub>	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V	1, 2, 3	All	3.5		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>BATT</sub> = 2.8 V unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
RESET AND WATCHDOG TIMING – continued							
RESET output voltage low	R <sub>VOL</sub>	I <sub>SINK</sub> = 1.6 mA	1	All		0.4	V
		I <sub>SINK</sub> = 800 μA	2, 3			0.4	
Output short circuit current	I <sub>OS</sub>	$\overline{\text{RESET}}$ , RESET, WDO, LL	1, 2, 3	All	1	25	μA
WDI input threshold logic low	WDI <sub>VIL</sub>	V <sub>CC</sub> = 5 V 3/ 4/	1	All		0.8	V
			2, 3			0.4	
WDI input threshold logic high	WDI <sub>VIH</sub>	V <sub>CC</sub> = 5 V 3/ 4/	1	All	3.5		V
			2, 3		4.0		
WDI input current	WDI <sub>IN</sub>	WDI = V <sub>OUT</sub>	1	All		50	μA
			2, 3			80	
		WDI = 0 V	1			-50	
			2, 3			-80	

POWER FAIL DETECTOR

PFI input threshold	PFI <sub>VTH</sub>	V <sub>CC</sub> = +5 V 3/	1, 2, 3	All	1.2	1.4	V
PFI input current	PFI <sub>IN</sub>		1, 2, 3	All	-25	+25	nA
$\overline{\text{PFO}}$ output voltage high	$\overline{\text{PFO}}$ <sub>VOH</sub>	I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 5 V	1, 2, 3	All	3.5		V
$\overline{\text{PFO}}$ output voltage low	$\overline{\text{PFO}}$ <sub>VOL</sub>	I <sub>SINK</sub> = 3.2 mA	1	All		0.4	V
		I <sub>SINK</sub> = 1.6 mA	2, 3			0.4	
$\overline{\text{PFO}}$ short circuit source current	$\overline{\text{PFO}}$ <sub>IOS</sub>	PFI = V <sub>IH</sub> , $\overline{\text{PFO}}$ = 0 V	1, 2, 3	All	1	25	μA

CHIP ENABLE GATING

$\overline{\text{CE}}$ <sub>IN</sub> thresholds logic low	$\overline{\text{CE}}$ <sub>VIL</sub>		1	All		0.8	V
			2, 3			0.4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>A</sub> ≤ +125°C V <sub>BATT</sub> = 2.8 V unless otherwise specified	Group A subgroup s	Device type	Limits <sup>2/</sup>		Unit
					Min	Max	
CHIP ENABLE GATING - continued							
$\overline{CE}$ IN thresholds logic high	$\overline{CE}$ VIH		1	All	3.0		V
			2, 3		4.0		
$\overline{CE}$ IN pullup current	$\overline{CE}$ INPI		1, 2, 3	All	1	25	μA
$\overline{CE}$ OUT output voltage high	$\overline{CE}$ VOH	I <sub>SOURCE</sub> = 3.0 mA, V <sub>CC</sub> = 4.75 V	1, 2, 3	All	V <sub>OUT</sub> -1.5		V
		I <sub>SOURCE</sub> = 1 μA, V <sub>CC</sub> = 0 V			V <sub>OUT</sub> -0.05		
$\overline{CE}$ OUT output voltage low	$\overline{CE}$ VOL	I <sub>SINK</sub> = 3.2 mA	1	All		0.4	V
		I <sub>SINK</sub> = 1.6 mA	2, 3			0.4	
$\overline{CE}$ propagation delay	t <sub>PDCE</sub>	V <sub>CC</sub> = 5 V	9	All		200	ns
			10, 11			300	

OSCILLATOR

OSC IN input pullup current	OSCIN <sub>IN</sub>		1, 2, 3	All		25	μA
OSC SEL input pullup current	OSCSEL <sub>IN</sub>		1, 2, 3	All	1	25	μA
OSC IN frequency range	OSCIN <sub>FRQ</sub>	OSC SEL = 0 V	9, 10, 11	All	0	250	kHz
OSC IN frequency with external capacitor	OSCIN	OSC SEL = 0 V, COSC = 47 pF, T <sub>A</sub> = +25°C <sup>5/</sup>	9	All	4		kHz

<sup>1/</sup> For device types 01 and 03, V<sub>CC</sub> = 4.75 V to 5.5 V, unless otherwise specified. For device type 02, V<sub>CC</sub> = 4.5 V to 5.5 V, unless otherwise specified.

<sup>2/</sup> The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used for these limits.

<sup>3/</sup> The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10 mA.

<sup>4/</sup> WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V<sub>CC</sub> is in the operating voltage range. WDI is internally biased to 38 percent of V<sub>CC</sub> with an impedance of approximately 125 kΩ.

<sup>5/</sup> Guaranteed, if not tested.

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Device type	01, 02, 03	01, 02
Case outline	E	2
Terminal number	Terminal symbol	
1	V <sub>BATT</sub>	N/C
2	V <sub>OUT</sub>	V <sub>BATT</sub>
3	V <sub>CC</sub>	V <sub>OUT</sub>
4	GND	V <sub>CC</sub>
5	BATT ON	GND
6	LOW LINE	N/C
7	OSC IN	BATT ON
8	OSC SEL	LOW LINE
9	PFI	OSC IN
10	PFO	OSC SEL
11	WDI	N/C
12	CE <sub>OUT</sub>	PFI
13	CE <sub>IN</sub>	PFO
14	WDO	WDI
15	RESET	CE <sub>OUT</sub>
16	RESET	N/C
17	----	CE <sub>IN</sub>
18	----	WDO
19	----	RESET
20	----	RESET

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-90711</b>
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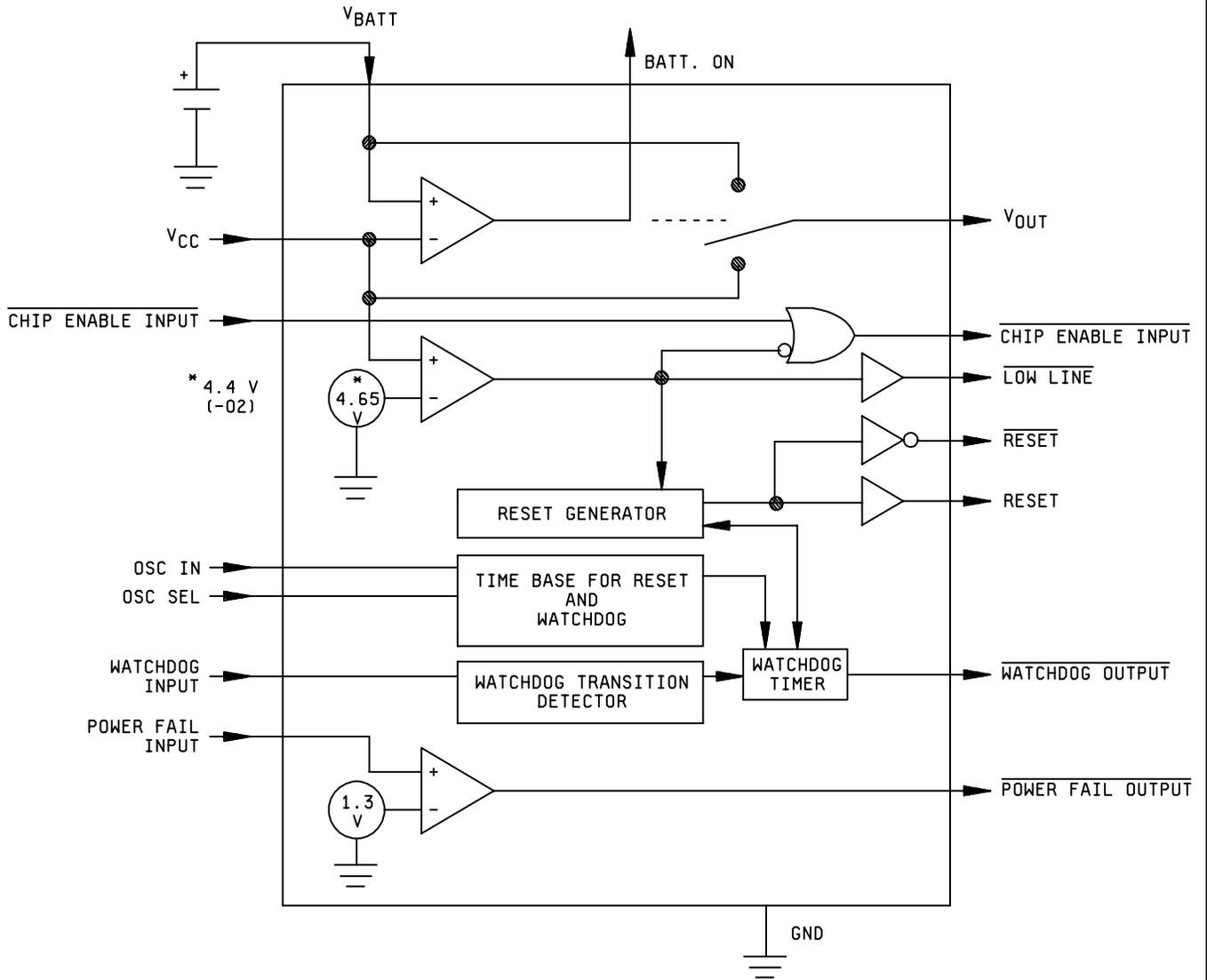


FIGURE 2. Block diagram.

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COLUMBUS, OHIO 43218-3990

SIZE  
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**A**

SHEET  
**10**

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1, 2, 3, <u>1/</u> 9, 10, 11	1, 2, 3, <u>1/</u> 9, 10, 11	1, 2, 3, <u>1/</u> 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3 9, 10, 11	1, 2, 3, 9, 10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 9	1, 9	1, 2, 3, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 9	1, 9	1, 9
Group E end-point electrical parameters (see 4.4)	-----	-----	-----

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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