

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device type 02. Editorial changes throughout.	92-09-24	M. A. FRYE
B	Add case outline F. Make changes to 1.2.2, 1.3, and FIGURE 1. Changes in accordance with N.O.R. 5962-R066-94.	93-12-16	M. A. FRYE
C	Add case outline E. Make changes to 1.2.2, 1.3, FIGURE 1, and editorial changes throughout. Redrawn.	97-11-13	R. MONNIN
D	Replaced reference to MIL-STD-973 with reference to MIL-PRF-38535. Drawing updated to reflect current requirements. -rrp	04-03-25	R. MONNIN

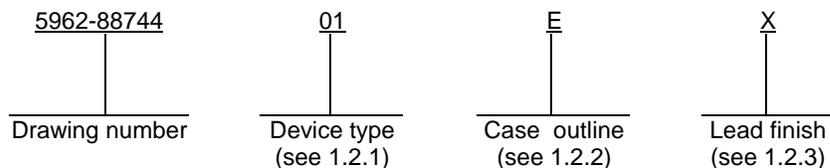


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REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12							
PMIC N/A	PREPARED BY RICK OFFICER		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsccl.dla.mil																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA																			
	APPROVED BY RAYMOND MONNIN		MICROCIRCUIT, LINEAR, DUAL DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON																	
	DRAWING APPROVAL DATE 91-02-07																			
	REVISION LEVEL D		SIZE A	CAGE CODE 67268	5962-88744															
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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	55113	Dual differential line driver with three state outputs
02	55114	Dual differential line driver with two state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage (V_{CC})	+7.0 V dc <u>1/</u>
Input voltage	+5.5 V dc
Off-state output voltage	+12.0 V dc
Maximum power dissipation (P_D):	
Cases E and 2	1375 mW <u>2/</u>
Case F	1000 mW <u>2/</u>
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	90°C/W
Case F	165°C/W
Case 2	65°C/W

1/ All voltage values are with respect to network ground terminal.

2/ With T_A above +25°C, the derating factors are 8.0°C/W for case F and 11.0°C/W for cases E and 2.

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1.4 Recommended operating conditions.

Supply voltage (V _{CC})	+4.5 V dc to +5.5 V dc
Ambient operating temperature range (T _A)	-55°C to +125°C
Minimum high level input voltage (V _{IH})	2.0 V dc
Maximum low level input voltage (V _{IL})	0.8 V dc
Maximum low level output current (I _{OL})	40 mA
High level output current (I _{OH})	-40 mA

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dia.mil/quicksearch/> or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Timing waveforms(s). The timing waveform(s) shall be as specified on figures 3, 4, and 5.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _A ≤ +125°C unless otherwise specified		Device types	Group A subgroups	Limits		Unit	
						Min	Max		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 40 mA		All	1, 2, 3		0.4	V	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IH} = 2 V, V _{IL} = 0.8 V	I _{OH} = -10 mA	All	1, 2, 3		2.4	V	
			I _{OH} = -40 mA				2.0		
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V, I _{IN} = -12 mA		All	1, 2, 3		-1.5		
Low level input current	A,B,C	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	All	1, 2, 3		-1.6	mA	
	CC			01			-3.2		
High level input current	A,B,C	I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	All	1, 2, 3		40	μA	
	CC			01			80		
Output clamp voltage	V _{OK}	V _{CC} = 5.5 V, I _O = -40 mA		01	1,2,3		-1.5	V	
				02	1		-1.5		
		V _{CC} = 5.0 V, I _O = +40 mA		02	1		6.5		
Supply current	I _{CC}	All inputs at 0 V, no load	V _{CC} = 5.5 V	01	1, 2, 3		65	mA	
			V _{CC} = 7.0 V				85		
			V _{CC} = 5.5 V	02	1, 2, 3		50		
			V _{CC} = 7.0 V				65		
Off-state (high impedance) output current	I _{OZ}	V _{CC} = 5.5 V, Output controls at 0.8 V	V _O = 0 V to V _{CC}	01	1		±10	μA	
			V _O = 0 V				2		-150
			V _O = 0.4 V				2		±80
			V _O = 2.4 V				2		±80
			V _O = V _{CC}				2		80

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified		Device types	Group A Subgroups	Limits		Unit
						Min	Max	
Off-state (open-collector) output current	I _{O(OFF)}	V _{CC} = 5.5 V, V _{OH} = 12 V		01	1		10	μA
				02			100	
				All	2		200	
Input current at maximum input voltage	I _I	V _{CC} = 5.5 V	A, B, C	All	1, 2, 3		1	mA
			CC	01			2	
Short circuit output current	I _{OS}	V _{CC} = 5.5 V, V _{OUT} = 0 V, T _A = 25°C		All	1	-40	-120	mA
Functional test		See 4.3.1.c		All	7, 8			
Propagation delay time	t _{PLH}	T _A = +25°C, V _{CC} = 5 V, C _L = 30 pF, see figure 3		All	9		20	ns
	t _{PHL}						20	
Output enable time to high level	t _{PZH}	R _L = 180 Ω, T _A = +25°C, V _{CC} = 5 V, C _L = 30 pF, See figure 4		01	9		15	ns
Output enable time to low level	t _{PZL}	R _L = 250 Ω, T _A = +25°C, V _{CC} = 5 V, C _L = 30 pF, See figure 5		01	9		30	ns
Output disable time from high level	t _{PHZ}	R _L = 180 Ω, T _A = +25°C, V _{CC} = 5 V, C _L = 30 pF, See figure 4		01	9		20	ns
Output disable time from low level	t _{PLZ}	R _L = 250 Ω, T _A = +25°C, V _{CC} = 5 V, C _L = 30 pF, See figure 5		01	9		35	ns

^{1/} All parameters, with the exception of off-state open collector output current (I_{O(OFF)}), are measured with the active pull-up connected to the sink output.

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Device types	01		02	
Case outlines	E and F	2	E and F	2
Terminal number	Terminal symbol			
1	1ZP	NC	1ZP	NC
2	1ZS	1ZP	1ZS	1ZP
3	1YS	1ZS	1YS	1ZS
4	1YP	1YS	1YP	1YS
5	1A	1YP	1A	1YP
6	1B	NC	1B	NC
7	1C	1A	1C	1A
8	GND	1B	GND	1B
9	CC	1C	2A	1C
10	2C	GND	2B	GND
11	2A	NC	2C	NC
12	2YP	CC	2YP	2A
13	2YS	2C	2YS	2B
14	2ZS	2A	2ZS	2C
15	2ZP	2YP	2ZP	2YP
16	V _{cc}	NC	V _{cc}	NC
17	---	2YS	---	2YS
18	---	2ZS	---	2ZS
19	---	2ZP	---	2ZP
20	---	V _{cc}	---	V _{cc}

FIGURE 1. Terminal connections.

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Device type 01

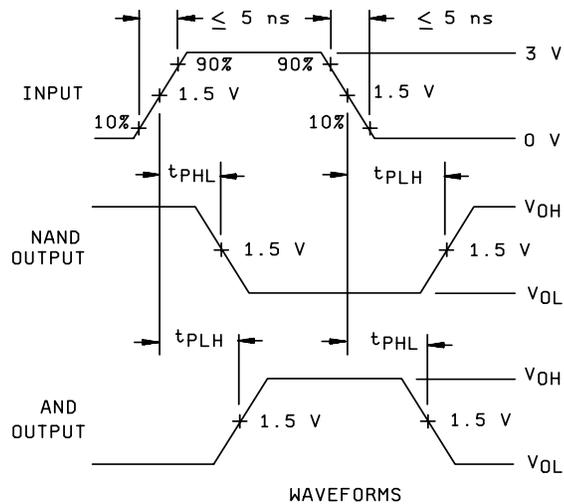
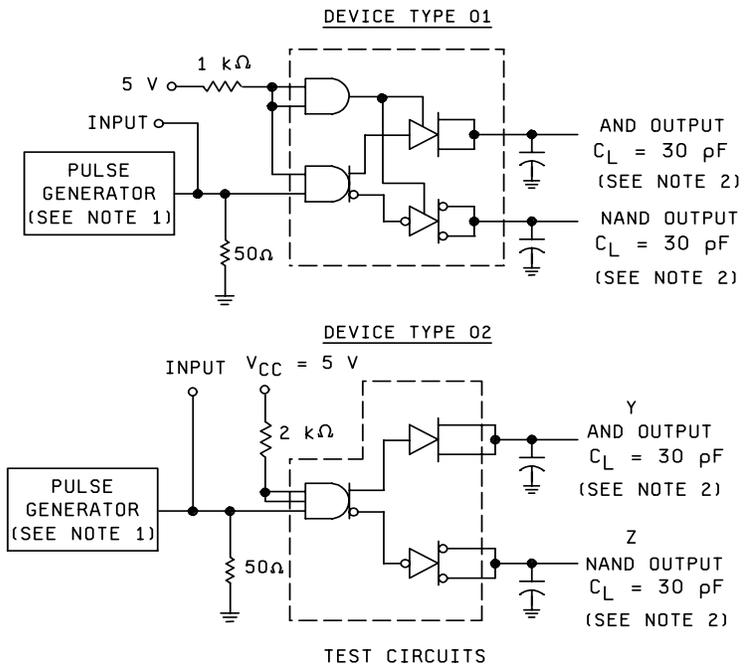
Inputs				Output			
1A or 2A	1B	1C or 2C	CC	ZP	ZS	YS	YP
L	L or H	H	H	H	Hi Z	L	Hi Z
L or H	L	H	H	H	Hi Z	L	Hi Z
H	H	H	H	Hi Z	L	Hi Z	H
L or H	L or H	L	L or H	Hi Z	Hi Z	Hi Z	Hi Z
L or H	L or H	L or H	L	Hi Z	Hi Z	Hi Z	Hi Z

Device type 02

Inputs			Outputs	
A	B	C	Y	Z
H	H	H	H	L
All other input combinations			L	H

FIGURE 2. Truth table.

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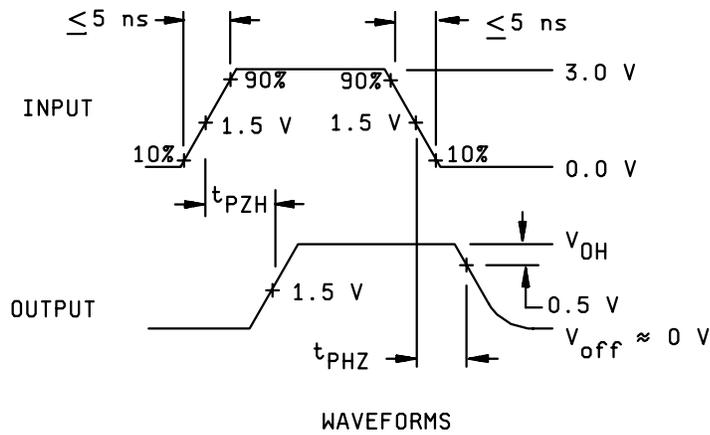
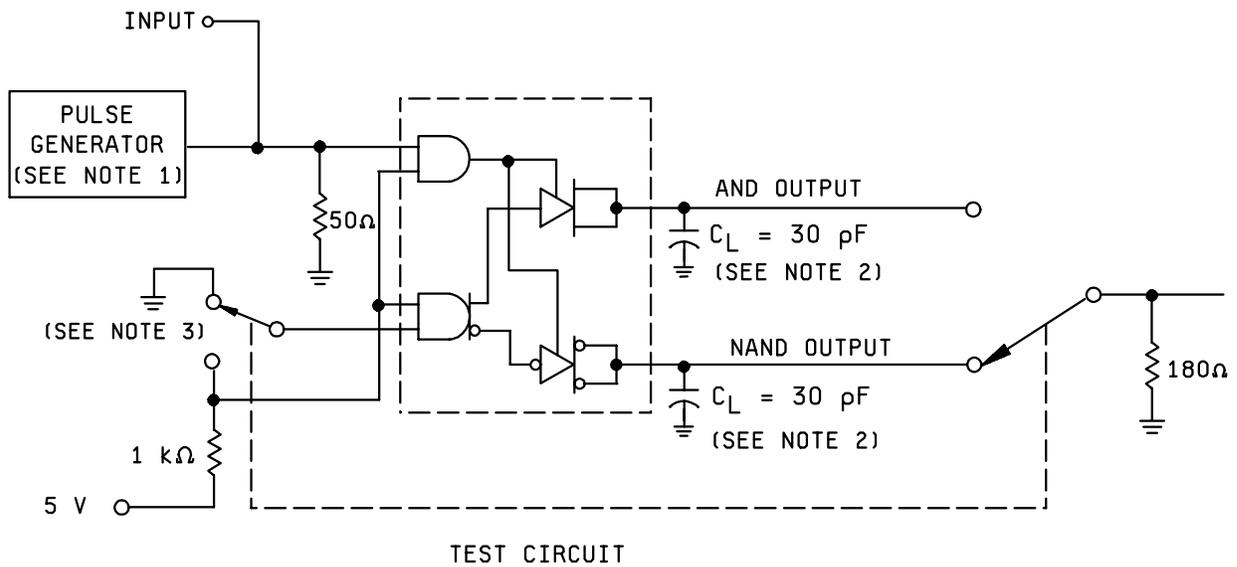
NOTES:

1. The pulse generator has the following characteristics $Z_O = 50 \Omega$, $PRR \leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$.
2. C_L includes probe and jig capacitance.

FIGURE 3. Waveforms and test circuit for low-to-high and high-to-low outputs.

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DEVICE TYPE 01



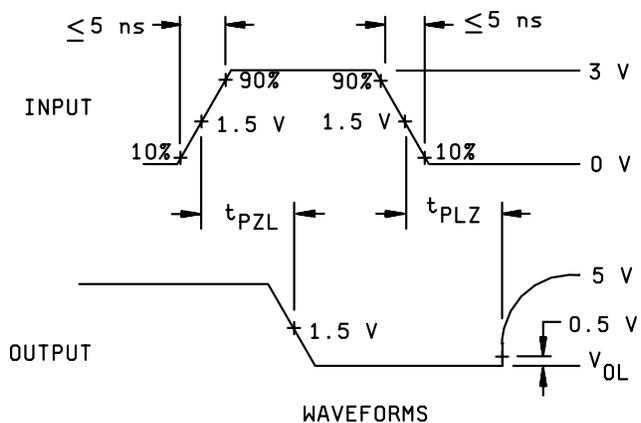
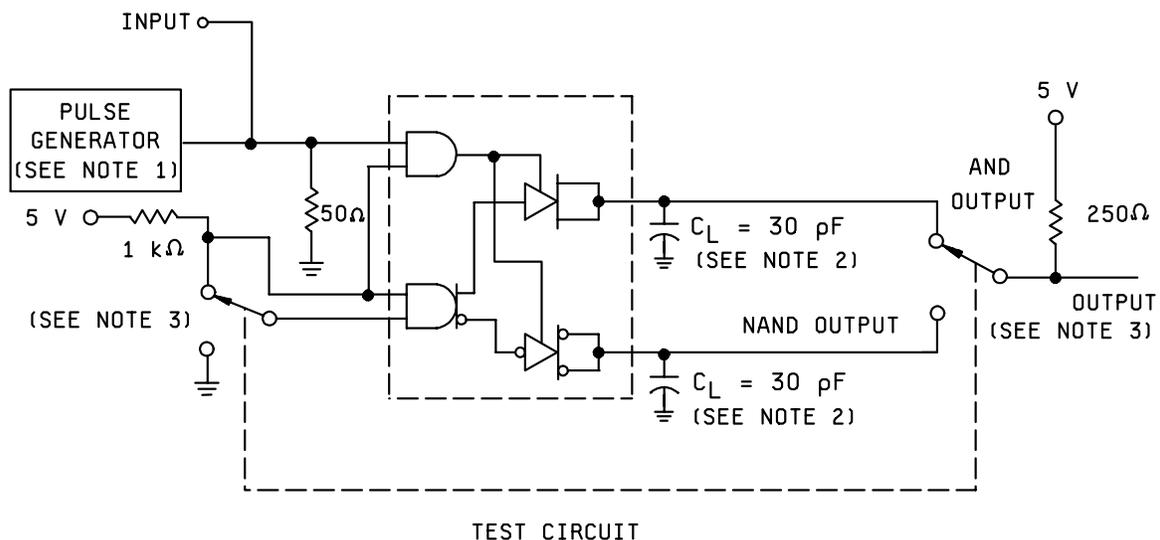
NOTES:

1. The pulse generator has the following characteristics $Z_o = 50 \Omega$, $PRR \leq 500 \text{ kHz}$, $t_w = 100 \text{ ns}$.
2. C_L includes probe and jig capacitance.
3. The parameter from table I is valid with the switch in either position.

FIGURE 4. Waveforms and test circuit for enable-to-high and high-to-disable.

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DEVICE TYPE 01



NOTES:

1. The pulse generator has the following characteristics $Z_O = 50 \Omega$, $PRR \leq 500 \text{ kHz}$, $t_w = 100 \text{ ns}$.
2. C_L includes probe and jig capacitance.
3. The parameter from table I is valid with the switch in either position.

FIGURE 5. Waveforms and test circuit for enable-to-low and low-to-disable outputs.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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