

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add the F-9 and F-10 packages to the drawing, also added vendor CAGE number 65786 to the drawing. Changes to table I, figure 1, and 6.4. Also added paragraph 4.3.3 to drawing. Editorial changes throughout.	89-01-27	D. R. Cool
B	Changes in accordance with NOR 5962-235-94.	94-07-26	Michael A. Frye
C	Update drawing to current requirements. Editorial changes throughout. – gap	01-04-03	Raymond Monnin

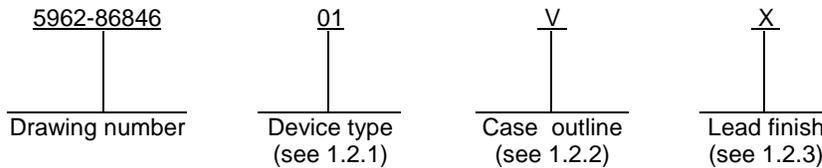
THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	C																		
SHEET	15																		
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY James E. Jamison		<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dscc.dla.mil</p> <p align="center">MICROCIRCUIT, DIGITAL, CMOS 64 X 5 PARALLEL FIFO, MONOLITHIC SILICON</p>																
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Ray Monnin																		
	APPROVED BY D. R. Cool																		
	DRAWING APPROVAL DATE 88-04-15																		
	REVISION LEVEL C	SIZE A	CAGE CODE 67268	5962-86846															
		SHEET		1 OF 15															

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Shift in/out rate</u>
01	72404L10	64 x 5 CMOS parallel FIFO	10 MHz
02	72404L15	64 x 5 CMOS parallel FIFO	15 MHz
03	72404L25	64 x 5 CMOS parallel FIFO	25 MHz
04	72404L35	64 x 5 CMOS parallel FIFO	35 MHz

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
S	GDFF-F20 or CDFF3-F20	20	Flat package
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
X	GDFF2-F18	18	Flat package
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) <u>1/</u>	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ _{JC}):	
Cases S, V, X, and 2	See MIL-STD-1835
Junction temperature (T _J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V _{CC})	4.5 V dc to 5.5 V dc
Supply voltage (GND)	0 V dc
Input high voltage (V _{IH})	2.0 V dc minimum
Input low voltage (V _{IL})	0.8 V dc maximum <u>2/</u>
Case operating temperature range (T _C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2/ -1.5 V undershoots are allowed for 10 ns once per cycle.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagrams. The block diagrams shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low current	I _{IL}	0 V ≤ V _{IN} ≤ 5.5 V, V _{CC} = 5.5 V	1, 2, 3	All	-10		μA
Input high current	I _{IH}	0 V ≤ V _{IN} ≤ 5.5 V, V _{CC} = 5.5 V	1, 2, 3	All		+10	μA
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8.0 mA V _{IL} = 0.8 V, V _{IH} = 2.0 V	1, 2, 3	All		0.4	V
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -4.0 mA V _{IL} = 0.8 V, V _{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output short-circuit current <u>1/</u>	I _{OS}	V _{CC} = 5.5 V, V _O = 0 V	1, 2, 3	All	-20	-110	mA
Off-state output high current	I _{HZ}	V _{CC} = 5.5 V, V _O = 2.4 V	1, 2, 3	All		+50	μA
Off-state output low current	I _{LZ}	V _{CC} = 5.5 V, V _O = 0.4 V	1, 2, 3	All	-50		μA
Operating supply current	I _{CC}	Inputs = V _{IH} outputs open	1, 2, 3	All		90	mA
Input capacitance	C _{IN}	V _{IN} = 0 V, f = 1.0 MHz, T _A = +25°C, see 4.3.1c	4	All		7.0	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V, f = 1.0 MHz, T _A = +25°C, see 4.3.1c	4	All		7.0	pF
Functional test		See 4.3.1d	7, 8	All			
Shift in rate	f _{IN}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01		10	MHz
				02		15	
				03		25	
				04		35	
Shift in to input ready low <u>3/</u>	t _{IRL}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01		40	ns
				02		35	
				03		22	
				04		18	
Shift in to input ready high <u>3/</u>	t _{IRH}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01		45	ns
				02		40	
				03		30	
				04		20	
Shift out rate	f _{OUT}	See figures 3 and 5 <u>2/</u>	9, 10, 11	01		10	MHz
				02		15	
				03		25	
				04		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shift out to output ready low <u>3/</u>	t _{ORL}	See figures 3 and 5 <u>2/</u>	9, 10, 11	01		40	ns
				02		35	
				03		21	
				04		18	
Shift out to output ready high <u>3/</u>	t _{ORH}	See figures 3 and 5 <u>2/</u>	9, 10, 11	01		55	ns
				02		40	
				03		37	
				04		20	
Output data hold (previous word) <u>4/</u>	t _{ODH}	See figures 3 and 5 <u>2/</u>	9, 10, 11	All	5.0		ns
Output data shift (next word)	t _{ODS}	See figures 3 and 5 <u>2/</u> , <u>5/</u>	9, 10, 11	01, 02		55	ns
				03		37	
				04		25	
Data throughput or "fall through" <u>4/</u>	t _{PT}	See figures 3, 6, and 7 <u>2/</u>	9, 10, 11	01, 02		65	ns
				03		60	
				04		28	
MASTER RESET to OR low	t _{MRORL}	See figures 3 and 8 <u>2/</u>	9, 10, 11	01		40	ns
				02, 03		35	
				04		28	
MASTER RESET to IR high <u>4/</u>	t _{MRIRH}	See figures 3 and 8 <u>2/</u>	9, 10, 11	01		40	ns
				02, 03		35	
				04		28	
MASTER RESET to data output low	t _{MRQ}	See figures 3 and 8 <u>2/</u>	9, 10, 11	01		40	ns
				02		35	
				03		25	
				04		20	
Output valid from OE low	t _{OOE}	See figures 3 and 9 <u>2/</u>	9, 10, 11	01		35	ns
				02		30	
				03		20	
				04		15	
Output high impedance from OE high <u>4/</u>	t _{HZOE}	See figures 3 and 9 <u>2/</u>	9, 10, 11	01		30	ns
				02		25	
				03		15	
				04		12	
Input ready pulse high <u>4/</u> , <u>5/</u>	t _{IPH}	See figures 3 and 6 <u>2/</u>	9, 10, 11	01, 02, 03	10		ns
				04	5.0		
Output ready pulse high <u>4/</u> , <u>5/</u>	t _{OPH}	See figures 3 and 7 <u>2/</u>	9, 10, 11	01, 02, 03	10		ns
				04	5.0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shift in high time <u>3/</u>	t _{SIH}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01, 02	20		ns
				03	11		
				04	9.0		
Shift in low time	t _{SIL}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01	30		ns
				02	25		
				03	24		
				04	17		
Input data setup time	t _{IDS}	See figures 3 and 4 <u>2/</u>	9, 10, 11	All	0		ns
Input data hold time	t _{IDH}	See figures 3 and 4 <u>2/</u>	9, 10, 11	01	40		ns
				02	30		
				03	20		
				04	15		
Shift out high time <u>3/</u>	t _{SOH}	See figures 3 and 5 <u>2/</u>	9, 10, 11	01, 02	20		ns
				03	11		
				04	9.0		
Shift out low time	t _{SOL}	See figures 3 and 5 <u>2/</u>	9, 10, 11	01	30		ns
				02	25		
				03	24		
				04	17		
MASTER RESET pulse width	t _{MRW}	See figures 3 and 8 <u>2/</u>	9, 10, 11	01	30		ns
				02, 03, 04	25		
MASTER RESET pulse to SI <u>4/</u>	t _{MRS}	See figures 3 and 8 <u>2/</u>	9, 10, 11	01	35		ns
				02	25		
				03, 04	10		
Data setup to IR <u>4/</u>	t _{SIR}	See figures 3 and 6 <u>2/</u>	9, 10, 11	01, 02, 03	5.0		ns
				04	3.0		
Data hold from IR <u>4/</u>	t _{HIR}	See figures 3 and 6 <u>2/</u>	9, 10, 11	01, 02	30		ns
				03	20		
				04	15		
Data setup to OR high <u>4/</u>	t _{SOR}	See figures 3 and 7 <u>2/</u>	9, 10, 11	All	0		ns

- 1/ Not more than one output should be shorted at a time. Duration of the short-circuit condition should not exceed one second. May not be tested, but shall be guaranteed to the limits specified in table I.
- 2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V.
- 3/ Since these devices are very high speed, care must be exercised in the design of the hardware and timing utilized in the design. Device grounding and decoupling are crucial to correct operation as the device will respond to very small glitches due to long reflective lines, high capacitances or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead lengths is recommended.
- 4/ May not be tested, but shall be guaranteed to the limits specified in table I.
- 5/ This parameter applies to devices communicating with each other in a cascaded mode.

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Device types	All		
Case outlines	V and X	S	2
Terminal number	Terminal symbol		
1	\overline{OE}	\overline{OE}	\overline{OE}
2	IR	NC	IR
3	SI	IR	NC
4	D ₀	SI	SI
5	D ₁	D ₀	D ₀
6	D ₂	D ₁	D ₁
7	D ₃	D ₂	D ₂
8	D ₄	D ₃	D ₃
9	GND	D ₄	D ₄
10	\overline{MR}	GND	GND
11	Q ₄	\overline{MR}	\overline{MR}
12	Q ₃	Q ₄	Q ₄
13	Q ₂	Q ₃	NC
14	Q ₁	Q ₂	Q ₃
15	Q ₀	Q ₁	Q ₂
16	OR	Q ₀	Q ₁
17	SO	OR	Q ₀
18	V _{CC}	SO	OR
19	---	NC	SO
20	---	V _{CC}	V _{CC}

FIGURE 1. Terminal connections.

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Device types 01 - 04

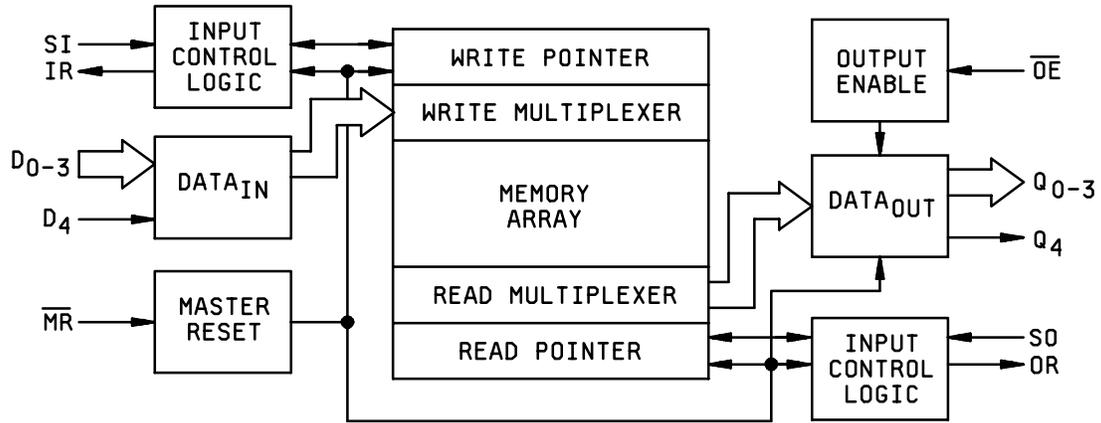
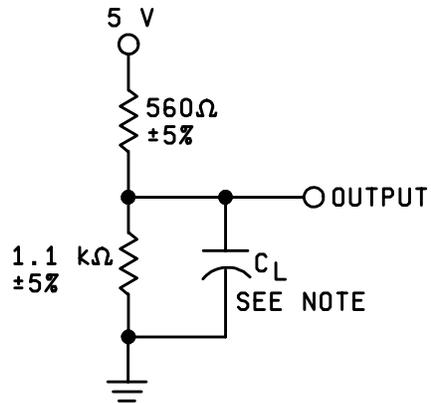


FIGURE 2. Block diagram.

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NOTE: $C_L = 5.0 \text{ pF}$ maximum for t_{HZOE} and t_{OOE} and $C_L = 30 \text{ pF}$ maximum for all other measurements. C_L includes jig and scope capacitance.

FIGURE 3. Output load circuit.

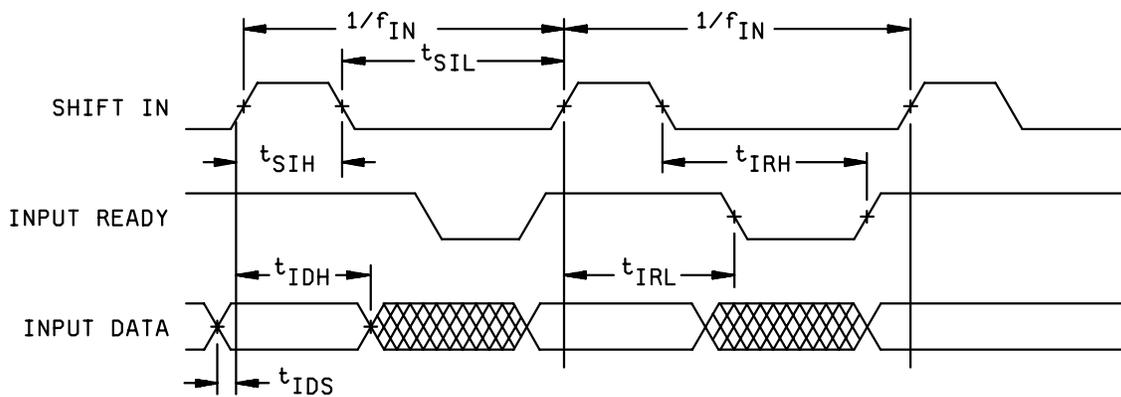
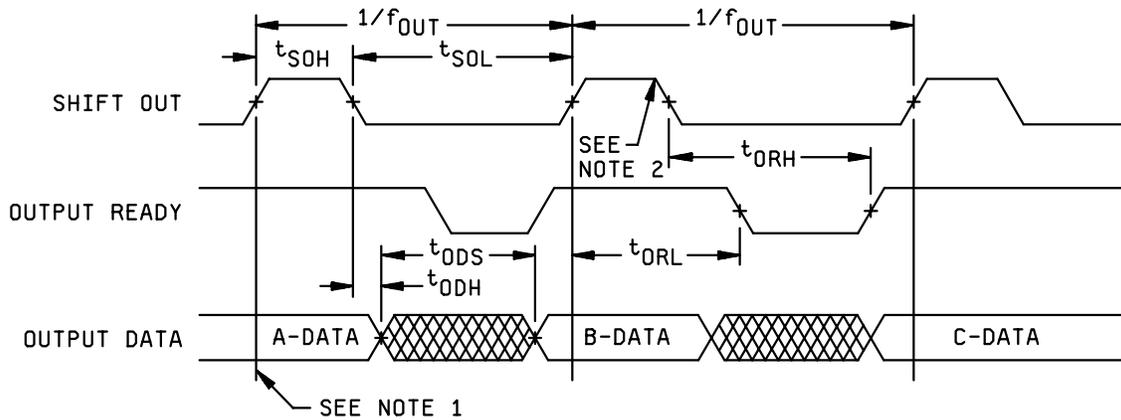


FIGURE 4. Input timing diagram.

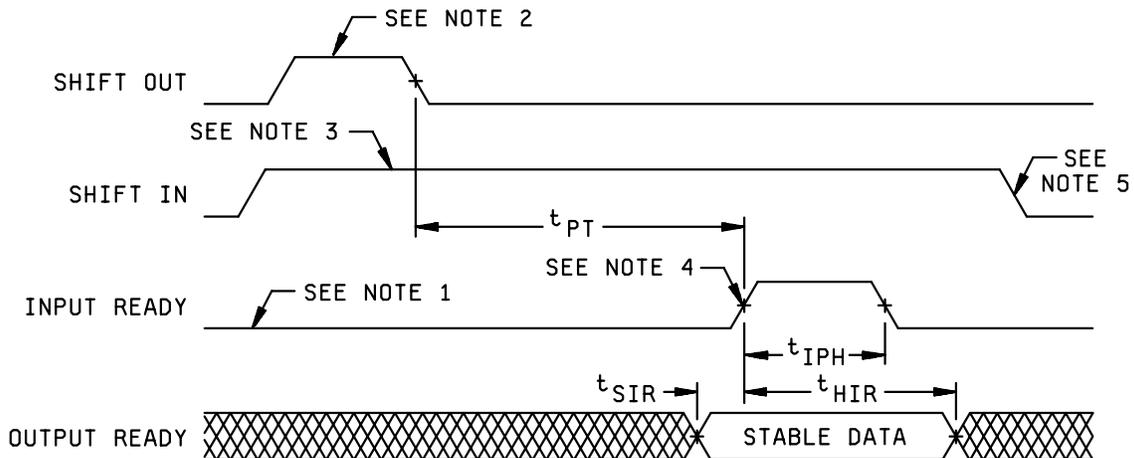
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NOTES:

1. This data is loaded consecutively, A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

FIGURE 5. Output timing diagram.

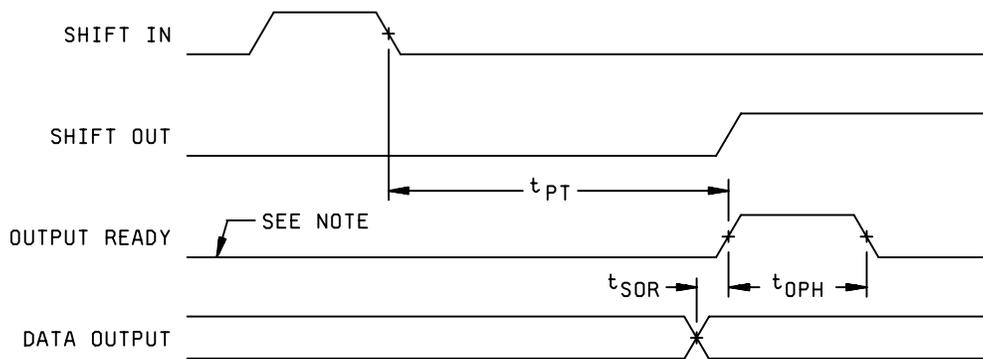


NOTES:

1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as input ready becomes HIGH the input data is loaded into the FIFO.
5. The write pointer is incremented.

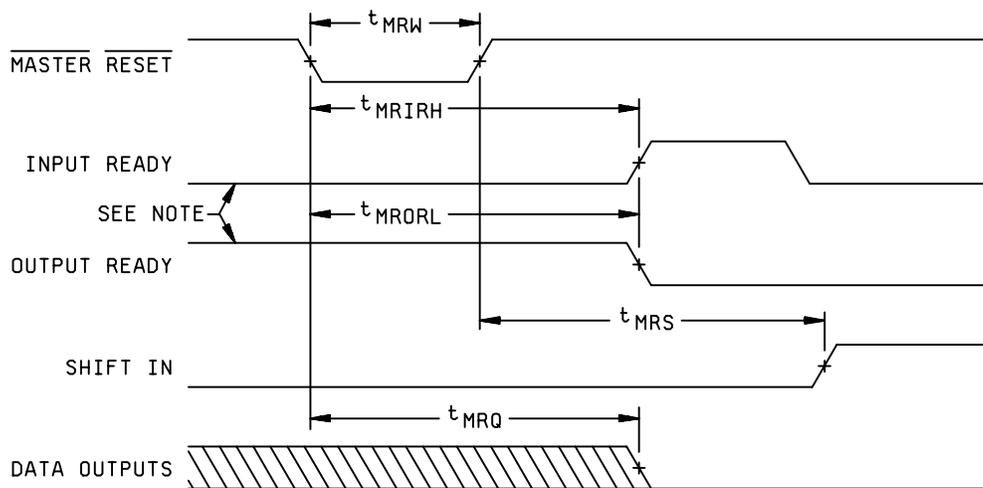
FIGURE 6. t_{IPH} , t_{HIR} , and t_{SIR} timing diagram.

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NOTE: FIFO initially empty.

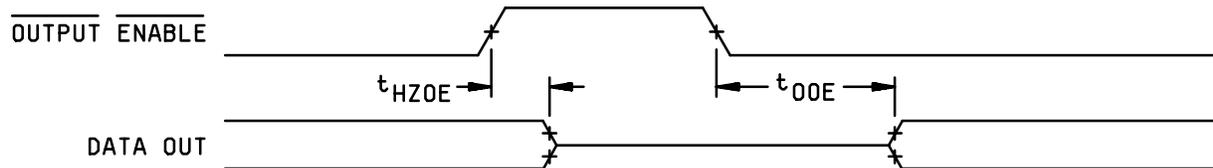
FIGURE 7. t_{PT} and t_{OPH} timing diagram.



NOTE: Worst case, FIFO initially full.

FIGURE 8. Master RESET timing.

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NOTE: High Z transitions are referenced to the steady-state $V_{OH} - 500\text{ mV}$ and $V_{OL} + 500\text{ mV}$ Levels on the output.

FIGURE 9. Output enable timing.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroups 1 and 7.

** For subgroup 4, see 4.3.1c.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall be sufficient to verify the functional operation of the device. It forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-86846
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