

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete t _{pd18} , t _{pd22} , and t _{pd27} from table I. Add footnote 2/. Convert to military drawing format. Editorial changes throughout.	1986 OCT 27	M. A. Frye
B	Change code identification number to 67268. Add vendor CAGE number 50088 as a second source. Editorial changes throughout.	1987 NOV 12	M. A. Frye
C	Changes to table I. Editorial change throughout	1988 OCT 7	M. A. Frye

CURRENT CAGE CODE 67268

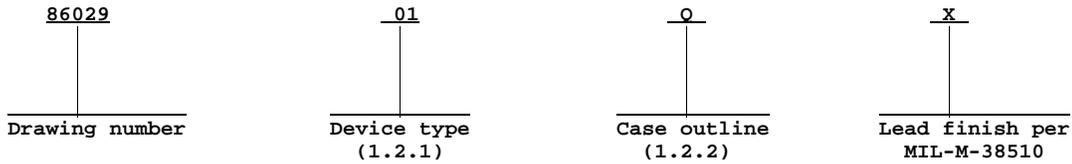
REV																				
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REV STATUS OF SHEETS				REV		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
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PMIC N/A <p style="text-align: center;">STANDARDIZED MILITARY DRAWING</p> THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Greg A. Pitz CHECKED BY Ray Monnin APPROVED BY Michael A. Frye DRAWING APPROVAL DATE 24 FEBRUARY 1986 REVISION LEVEL <p style="text-align: center;">C</p>	<p>DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p> <p>MICROCIRCUIT, VECTORED PRIORITY INTERRUPT CONTROLLER, MONOLITHIC SILICON</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <tr> <td style="width: 15%;">SIZE</td> <td style="width: 35%;">CAGE CODE</td> <td style="width: 50%; text-align: center;">86029</td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">14933</td> <td></td> </tr> </table> <p style="margin-top: 10px;">SHEET 1 OF 19</p>	SIZE	CAGE CODE	86029	A	14933	
SIZE	CAGE CODE	86029						
A	14933							

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	2914	Bipolar vectored priority interrupt controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
Q	D-5 (40-lead, 2.096" x .620" x .225") dual-in-line package
U	C-5 (44-terminal, .662" x .662" x .120") square chip carrier package
Y	See figure 1 (42-lead, 1.090" x .660" x .115") flat package

1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range- - - - -	-0.5 V dc to +5.5 V dc
Storage temperature range- - - - -	-65°C to +150°C
Maximum power dissipation (P_D) <u>1/</u> - - - - -	1.705 W
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q and U - - - - -	(See MIL-M-38510, appendix C)
Case Y - - - - -	40°C/W
Junction temperature (T_J)- - - - -	+175°C
DC output current, into inputs - - - - -	30 mA
DC input current - - - - -	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) - - - - -	2.0 V dc
Maximum low level input voltage (V_{IL})- - - - -	0.8 V dc
Case operating temperature range (T_C)- - - - -	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test e.g., I_{OS} .

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 2

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Block diagram. The block diagram shall be as specified on figure 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Instruction set. The instruction set shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 3

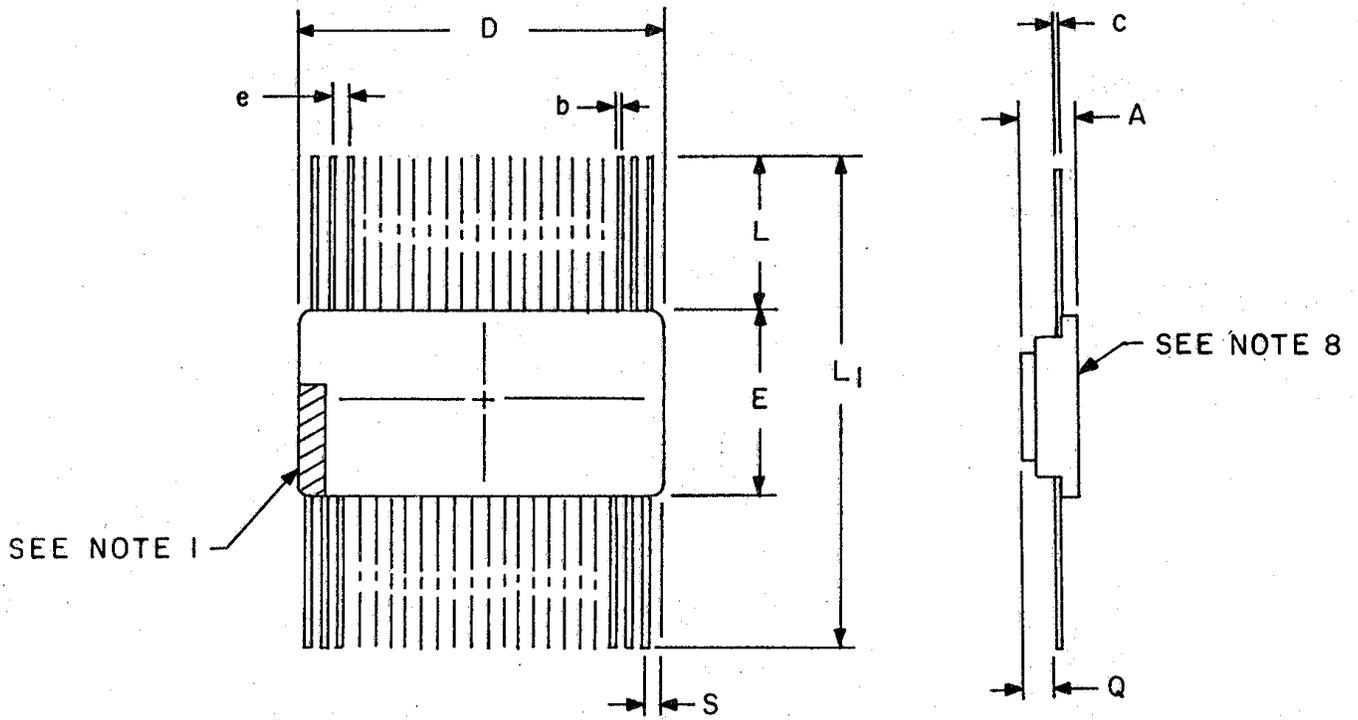


FIGURE 1. Case outline Y (42-lead, 1.090" x .660").

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

86029

REVISION LEVEL
C

SHEET
4

Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.070	.115	1.78	2.92	
b	.017	.023	0.43	0.58	5
c	.006	.012	0.15	0.30	5
D	1.030	1.090	26.16	27.69	
E	.600	.660	15.24	16.76	
E1	---	.720	---	18.29	3
e	.045	.055	1.14	1.40	4, 6
L	.250	.370	6.35	9.40	
L1	1.300	1.370	33.02	34.80	
Q	.020	.060	0.51	1.52	2
S	.005	---	0.13	---	7

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within ± 0.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 42.
5. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Forty spaces.
7. Applies to all four corners (lead numbers 1, 21, 22, and 42).
8. Configuration 2 is optional. If this configuration is used, no organic or polymeric materials shall be molded to the top of the package to cover the leads.

FIGURE 1. Case outline Y (42-lead, 1.090" x .660". - Continued

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 5

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output high voltage	V _{OH}	V _{CC} = Minimum, I _{OH} = -1.0 mA V _{IN} = V _{IH} or V _{IL}	1, 2, 3	2.4		V
Output low voltage	V _{OL}	V _{CC} = Minimum V _{IN} = V _{IH} or V _{IL}	1, 2, 3		0.4	V
					0.45	
					0.5	
Input high level	V _{IH}		1, 2, 3	2.0		V
Input low level	V _{IL}		1, 2, 3		0.8	V
Input clamp voltage	V _{IC}	V _{CC} = Minimum, I _{IN} = -18 mA	1, 2, 3		-1.5	V
Output leakage current for IR output	I _{CEX}	V _{CC} = Minimum, V _O = 5.5 V	1, 2, 3		250	µA
Input low current	I _{IL}	V _{CC} = Maximum V _{IN} = 0.4 V	1, 2, 3	M _{O-7}	-0.15	mA
				S _{O-2}	-0.1	
				LB	-0.4	
				ID	-2.0	
				IE	-1.2	
				All others	-0.8	
Input high current	I _{IH1}	V _{CC} = Maximum V _{IN} = 2.7 V	1, 2, 3	M _{O-7}	150	µA
				S _{O-2}	100	
				GE, GAR	40	
				IE	60	
				ID	60	
				All others	20	
Input high current	I _{IH2}	V _{CC} = Maximum, V _{IN} = 5.5 V	1, 2, 3		1.0	mA

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Off-state output current	I _{OZL}	V _{CC} = Maximum	V _{OUT} = 0.5 V	M _{O-7}	1, 2, 3	-150	mA
				S _{O-2}		-100	
				V _{O-2}		-50	
	I _{OZH}		V _{OUT} = 2.4 V	M _{O-7}		150	
				S _{O-2}		100	
				V _{O-2} others		50	
Power supply current	I _{CC}	V _{CC} = Maximum	-55°C, +25°C	1, 3	310	mA	
			+125°C	2	260		
<u>Functional tests</u>		See 4.3.1c		7, 8			
Output short circuit current <u>1</u> /	I _{OS}	V _{CC} = 6.0 V, V _O = 0.5 V		1, 2, 3	-30	-85	mA
Propagation delay from input IE to output:		See figure 5 <u>2</u> /		9, 10, 11			
SM Bus	t _{pd1}				60	ns	
S Bus	t _{pd2}				68	ns	
V ₀ , V ₁ , V ₂	t _{pd3}				70	ns	
<u>GAS</u>	t _{pd4}				62	ns	
Propagation delay from input I ₀ , I ₁ , I ₂ , I ₃ to output: SM Bus							
S Bus	t _{pd5}				60	ns	
V ₀ , V ₁ , V ₂	t _{pd6}				68	ns	
<u>GAS</u>	t _{pd7}				70	ns	
	t _{pd8}				62	ns	

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit	
				Min	Max		
Propagation delay from input IRPT disable to output: V ₀ , V ₁ , V ₂	t _{pd9}	See figure 5 2/	9, 10, 11		48	ns	
	t _{pd10}				60	ns	
	t _{pd11}				22	ns	
	t _{pd12}				33	ns	
Propagation delay from IRPT latches and register to: V ₀ , V ₁ , V ₂	t _{pd13}					82	ns
	t _{pd14}					105	ns
	t _{pd15}					75	ns
	t _{pd16}					75	ns
	t _{pd17}					85	ns
Propagation delay from mask register to:	t _{pd19}					105	ns
	t _{pd20}					75	ns
	t _{pd21}					75	ns
Propagation delay from status register to: V ₀ , V ₁ , V ₂	t _{pd23}					73	ns
	t _{pd24}					96	ns
	t _{pd25}					66	ns
	t _{pd26}					66	ns

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 8

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay from lowest group enabled flip-flop to: PD RD GS	t _{pd28}	See figure 5 2/	9, 10, 11		54	ns
	t _{pd29}				58	ns
	t _{pd30}				45	ns
Propagation delay from IRPT request enable flip-flop to IR	t _{pd31}				66	ns
Propagation delay from status over- flow flip-flop to status overflow	t _{pd32}				40	ns

See footnotes at end of table.

<p align="center">STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</p>	<p align="center">SIZE A</p>		<p align="center">86029</p>
		<p align="center">REVISION LEVEL C</p>	<p align="center">SHEET 9</p>

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time 1	from: S Bus	t _{s1}	9, 10, 11	15		ns
Hold time 1		t _{h1}		19		ns
Setup time 2	from: M Bus	t _{s2}		15		ns
Hold time 2		t _{h2}		16		ns
Setup time 3	from: P ₀ -P ₇	t _{s3}		15		ns
Hold time 3		t _{h3}		9		ns
Setup time 4	from: Latch bypass	t _{s4}		20		ns
Hold time 4		t _{h4}		0		ns
Setup time 5	from: IE, I ₀ , I ₁ , I ₂ , I ₃	t _{s5}		55 t _{PWL} +40		ns
Hold time 5	3/	t _{h5}		0		ns
Setup time 6	from: GE	t _{s6}		15		ns
Hold time 6		t _{h6}		13		ns
Setup time 7	from: GAR	t _{s7}		15		ns
Hold time 7		t _{h7}		17		ns
Setup time 8	from:	t _{s8}		42		ns
Hold time 8	ID	t _{h8}		14		ns

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 10

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V ±10% unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Hold time 9 from: $\overline{P_0}$ - $\overline{P_7}$ Hold time relative to LB	t _{h9}	See figure 5 2/	9, 10, 11	25		ns
Minimum clock low time	t _{pw1}			30		ns
Minimum clock high time	t _{pw2}			30		ns
Minimum interrupt input ($\overline{P_0}$ - $\overline{P_7}$) low time for guaranteed acceptance (pulse mode)	t _{pw3}			40		ns
Maximum interrupt input ($\overline{P_0}$ - $\overline{P_7}$) low time for guaranteed rejection (pulse mode)	t _{pw4}				8	ns
Minimum clock period, $\overline{IE} = H$ on current cycle and previous cycle	t _{pw5}			55		ns
Minimum clock period, $\overline{IE} = L$ on current cycle or previous cycle	t _{pw6}			110		ns

1/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed 1 second.

2/ All outputs fully loaded, C_L = 50 pF. Measurements made at 1.5 V with input levels of 0 and 3.0 V.

3/ t_{PWL} is the clock low time. Both setup times must be met.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 11

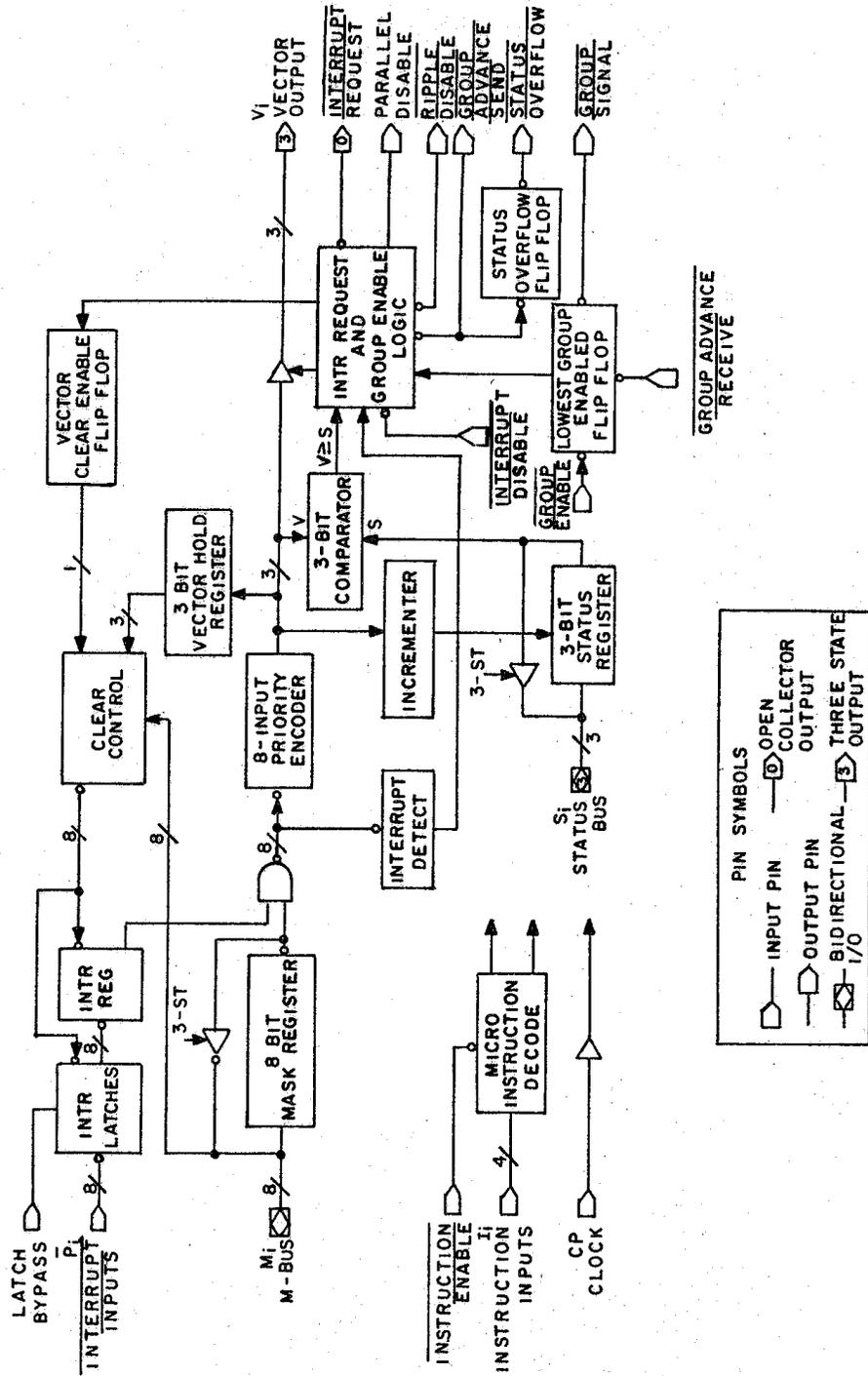


FIGURE 2. Block diagram.

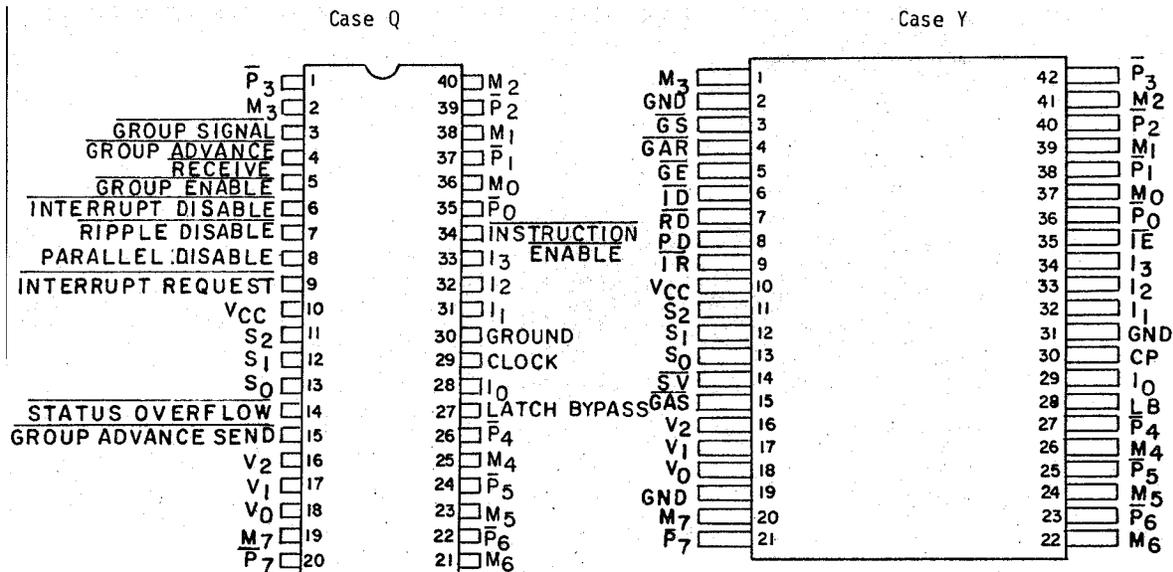
STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

86029

REVISION LEVEL
C

SHEET
12



NOTE: GND'S AND PINS 2, 19, & 31 MUST ALL BE TIED TOGETHER EXTERNALLY

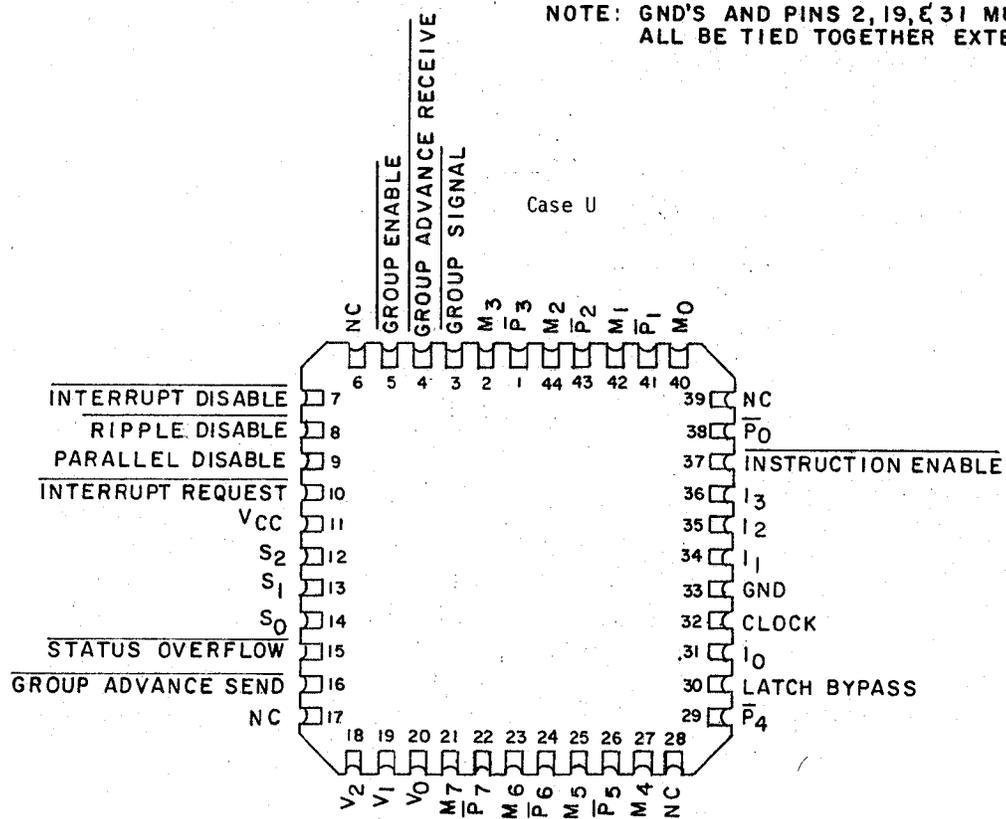


FIGURE 3. Terminal connections.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

86029

REVISION LEVEL
C

SHEET
13

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Mnemonic

Instruction

		Mask register functions
1110	LDM	Load mask register from M bus
0111	RDM	Read mask register to M bus
1100	CLRM	Clear mask register (enables all priorities)
1000	SETM	Set mask register (inhibits all interrupts)
1010	BCLRM	Bit clear mask register from M bus
1011	BSETM	Bit set mask register from M bus
		Status register functions
1001	LDSTA	Load status register from S bus and LGE flip-flop from $\overline{\text{GE}}$ input
0110	RDSTA	Read status register to S bus
		Interrupt request control
1111	ENIN	Enable interrupt request
1101	DISIN	Disable interrupt request
		Vectored output
0101	RDVC	Read vector output to V outputs, load V + 1 into status register, load V into vector hold register and set vector clear enable flip-flop
		Priority interrupt register clear
0001	CLRIN	Clear all interrupts
0011	CLRMR	Clear interrupts from mask register data (uses the M bus)
0010	CLRMB	Clear interrupts from M bus data
0100	CLRVC	Clear the individual interrupt associated with the last vector read
		Master clear
0000	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request

FIGURE 4. Instruction set.

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DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

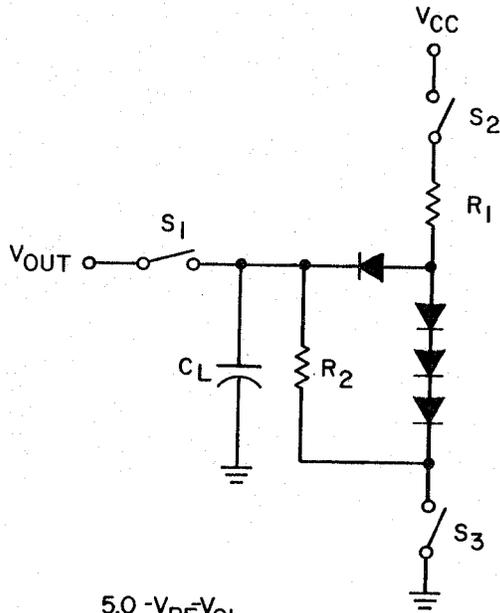
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REVISION LEVEL
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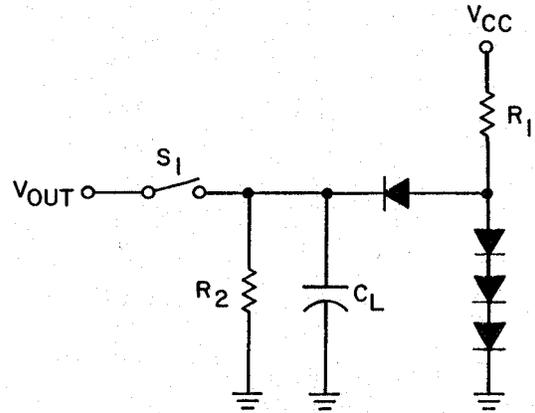
SHEET
14

A. Three-state outputs



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}} \cdot 1K$$

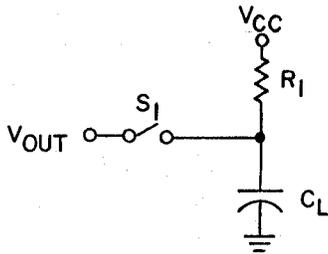
B. Normal outputs



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}} \cdot R_2$$

$$R_2 = \frac{2.4 V}{I_{OH}}$$

C. Open-collector outputs



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

FIGURE 5. Switching test circuit.

FIGURE 5. Switching test circuit.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

86029

REVISION LEVEL
C

SHEET
15

Test output load

Pin label	Test circuit	R1	R2
<u>Group</u> signal	B	300Ω	2.4 kΩ
<u>Group</u> advance receive	B	300Ω	2.4 kΩ
<u>Ripple</u> disable	B	300Ω	2.4 kΩ
Parallel disable	B	300Ω	2.4 kΩ
<u>Interrupt</u> request	C	390Ω	---
S ₀₋₂	A	300Ω	1 kΩ
<u>Status</u> overflow	B	300Ω	2.4 kΩ
V ₀₋₂	A	300Ω	1 kΩ
M ₀₋₇	A	300Ω	1 kΩ

NOTES:

1. C_L = 50 pF includes scope probe, stray wiring, and capacitances without device in test fixture.
2. S₁, S₂, and S₃ are closed during function tests and all ac tests except output enable tests.
3. S₁ and S₃ are closed while S₂ is open for enable high test. S₁ and S₂ are closed while S₃ is open for enable low test.
4. C_L = 5.0 pF for output disable tests.
5. Disable times measured from .5 V change on the output.

FIGURE 5. Switching test circuit - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 16

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroups 7 and 8 shall consist of verifying the instruction set.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		86029
		REVISION LEVEL C	SHEET 17

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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		REVISION LEVEL C	SHEET 18

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
8602901QX	34335 50088 50088	AM2914/BQA TS2914MCB/C TS2914MJB/C
8602901YX	34335	AM2914/BYC
8602901UX	34335 50088	AM2914/BUA TS2914MEB/C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34335

50088

Vendor name
and address

Advanced Micro Devices, Inc.
901 Thompson Place
P.O. Box 3453
Sunnyvale, CA 94088

Thomson Components-Mostek Corporation
1310 Electronics Drive
Carrollton, TX 75006

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		REVISION LEVEL C	SHEET 19