

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Converted to military drawing format. Add vendor CAGE number 50088 as second source. Changes Code Ident. No. to 67268.	87-11-07	R. P. Evans
D	Change I _{os} minimum limits in table I from -30 mA to -15 mA. Update boilerplate to MIL-PRF-38535 requirements. - CFS	03-08-04	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268.

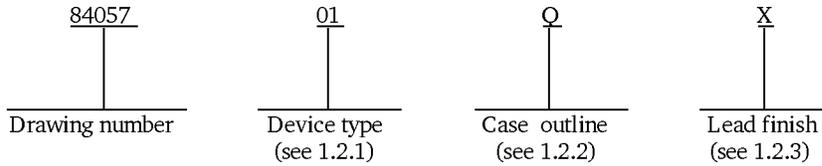
REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D										
SHEET	15	16	17	18	19	20	21	22	23	24										
REV STATUS	REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY James E. Jamison		<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.d.scc.dla.mil</p> <p align="center">MICROCIRCUIT, DIGITAL, FOUR-BIT MICROPROCESSOR SLICE, MONOLITHIC SILICON</p>																
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY D. A. DiCenzo																		
	APPROVED BY Robert P. Evans																		
	DRAWING APPROVAL DATE 84-08-01																		
	REVISION LEVEL D	SIZE A	CAGE CODE 14933	84057															
SHEET			1 OF 24																

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2901C	Four-bit microprocessor slice

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Z	See figure 1.	42	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings

Supply voltage range (V_{CC}).....	-0.5 V dc to +7.0 V dc
Input voltage range.....	-0.5 V dc to +5.5 V dc
Storage temperature range.....	-65 °C to +150 °C
Maximum power dissipation (P_D) $\frac{1}{2}$	1.6 W
Lead temperature (soldering, 10 seconds).....	+300 °C
Maximum junction temperature (T_J).....	+175 °C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q.....	See MIL-STD-1835
Case Z.....	9 °C/W

1.4 Recommended operating conditions

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH}).....	+2.0 V dc
Maximum low-level input voltage (V_{IL}).....	+0.8 V dc
Case operating temperature range (T_C).....	-55 °C to +125 °C

$\frac{1}{2}$ / Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 2

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 3

3.4 Electrical test requirements . The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking . Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark . A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance . A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance . A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change . Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review . DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 4

TABLE I. Electrical performance characteristics .

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage Y ₀ , Y ₁ , Y ₂ , Y ₃ , \overline{G}	V _{OH1}	V _{CC} =4.5 V, V _{IH} =2.0 V, V _{IL} =0.8 V	I _{OH} =-1.6 mA	1, 2, 3	All	2.4		V
High level output voltage OVR, \overline{P}	V _{OH2}		I _{OH} =-800 μA			2.4		
High level output voltage C _{n+4}	V _{OH3}		I _{OH} =-1.0 mA			2.4		
High level output voltage F ₃ , RAM ₀ , RAM ₃ , Q ₀ , Q ₃	V _{OH4}		I _{OH} =-600 μA			2.4		
Output leakage current for F =0 output	I _{CEX}	V _{CC} =4.5 V, V _{OH} =5.5 V V _{IH} =2.0 V, V _{IL} =0.8 V		1, 2, 3	All		250	μA
Low level output voltage Y ₀ , Y ₁ , Y ₂ , Y ₃ , \overline{G} , F =0	V _{OL1}	V _{CC} =4.5 V, V _{IH} =2.0 V, V _{IL} =0.8 V	I _{OL} =16 mA	1, 2, 3	All		0.5	V
Low level output voltage OVR, \overline{P}	V _{OL2}		I _{OL} =8.0 mA				0.5	
Low level output voltage C _{n+4}	V _{OL3}		I _{OL} =10 mA				0.5	
Low level output voltage F ₃ , RAM ₀ , RAM ₃ , Q ₀ , Q ₃	V _{OL4}		I _{OL} =6.0 mA				0.5	
Input clamp voltage	V _{IC}	V _{CC} =4.5 V, I _{IH} =-18 mA		1, 2, 3	All		-1.5	V
Low level input current Clock, \overline{OE} , I ₀ , I ₁ , I ₂ , I ₆ , I ₈	I _{IL1}	V _{CC} =5.5 V, V _{IN} =0.5 V		1, 2, 3	All		-0.36	mA
Low level input current A ₀ , A ₁ , A ₂ , A ₃ , B ₀ , B ₁ , B ₂ , B ₃	I _{IL2}						-0.36	
Low level input current D ₀ , D ₁ , D ₂ , D ₃	I _{IL3}						-0.72	
Low level input current I ₃ , I ₄ , I ₅ , I ₇	I _{IL4}						-0.72	
Low level input current RAM ₀ , RAM ₃ , Q ₀ , Q ₃	I _{IL5}						-0.8	
Low level input current C _n	I _{IL6}						-3.6	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level input current Clock, OE, A ₀ , A ₁ , A ₂ , A ₃ , B ₀ , B ₁ , B ₂ , B ₃ , I ₀ , I ₁ , I ₂ , I ₆ , I ₈	I _{IH1}	V _{CC} =5.5 V, V _{IN} =2.7 V		1, 2, 3	All		20	μA
High level input current D ₀ , D ₁ , D ₂ , D ₃ , I ₃ , I ₄ , I ₅ , I ₇	I _{IH2}						40	
High level input current RAM ₀ , RAM ₃ , Q ₀ , Q ₃	I _{IH3} <u>1/</u>						100	
High level input current C _n	I _{IH4}						200	
High impedance state output current Y ₀ , Y ₁ , Y ₂ , Y ₃	I _{ZH1} I _{ZL1}	V _{CC} =5.5 V	V _{OUT} =2.4 V	1, 2, 3	All		50	μA
High impedance state output current RAM ₀ , RAM ₃ , Q ₀ , Q ₃	I _{ZH2} <u>1/</u>		V _{OUT} =0.5 V				-50	
	I _{ZL2} <u>1/</u>		V _{OUT} =2.4 V				100	
			V _{OUT} =0.5 V				-800	
Output short circuit current	I _{OS} <u>2/</u>	V _{CC} =5.5 V, V _{OUT} =0 V	Y ₀ , Y ₁ , Y ₂ , Y ₃ , \overline{G} , C _{n+4} , OVR, P, F ₃ , RAM ₀ , RAM ₃ , Q ₀ , Q ₃	1, 2, 3	All	-15	-85	mA
Power supply current	I _{CC}	V _{CC} =5.5 V		1, 2, 3	All		280	mA
Frequency of operation	f _{MAX}			1, 2, 3	All	31		MHz
Functional tests		See 4.4.1c		7, 8	All			
A ₃ -A ₀ setup time to positive edge of clock	t _{SHL1} t _{SLH1}	C _L =50 ±5 pF all outputs. See figure 5.		9, 10, 11	All	30		ns
A ₃ -A ₀ setup time to negative edge of clock	t _{SHL2} t _{SLH2}					15		
	B ₃ -B ₀ (source) setup time to positive edge of clock					t _{SHL3} t _{SLH3}	30	
B ₃ -B ₀ (source) setup time to negative edge of clock						t _{SHL4} t _{SLH4}	15	
	B ₃ -B ₀ (DEST) setup time to negative edge of clock					t _{SHL5} t _{SLH5}	15	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _C +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
D ₃ -D ₀ (arithmetic mode) setup time to positive edge of clock	t _{SHL6}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All	25		ns
	t _{SLH6}				25		
D ₃ -D ₀ (I = X37) setup time to positive edge of clock	t _{SHL7}				25		
	t _{SLH7}				25		
C _n setup time to positive edge of clock	t _{SHL8}				20		
	t _{SLH8}				20		
I ₂ -I ₀ setup time to positive edge of clock	t _{SHL9}				30		
	t _{SLH9}				30		
I ₅ -I ₃ setup time to positive edge of clock	t _{SHL10}				30		
	t _{SLH10}				30		
I ₈ -I ₆ setup time to negative edge of clock	t _{SHL11}				10		
	t _{SLH11}				10		
Q ₃ , Q ₀ setup time to positive edge of clock	t _{SHL12}				12		
	t _{SLH12}				12		
RAM ₃ , RAM ₀ setup time to positive edge of clock	t _{SHL13}				12		
	t _{SLH13}				12		
A ₃ -A ₀ hold time from positive edge of clock	t _{HHL1}				2		
	t _{HLH1}				2		
B ₃ -B ₀ hold time from positive edge of clock	t _{HHL2}				2		
	t _{HLH2}				2		
D ₃ -D ₀ hold time from positive edge of clock	t _{HHL3}	0					
	t _{HLH3}	0					
C _n hold time from positive edge of clock	t _{HHL4}	0					
	t _{HLH4}	0					
I ₈ -I ₀ hold time from positive edge of clock	t _{HHL5}	0					
	t _{HLH5}	0					
Q ₃ , Q ₀ hold time from positive edge of clock	t _{HHL6}	0					
	t _{HLH6}	0					
RAM ₃ , RAM ₀ hold time from positive edge of clock	t _{HHL7}	0					
	t _{HLH7}	0					

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _C +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay from A ₃ -A ₀ to Y ₃ -Y ₀	t _{PHL1}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All		48	ns
	t _{PLH1}					48	
Delay from A ₃ -A ₀ to F ₃	t _{PHL2}					48	
	t _{PLH2}					48	
Delay from A ₃ -A ₀ to C _{n+4}	t _{PHL3}					48	
	t _{PLH3}					48	
Delay from A ₃ -A ₀ to G and P	t _{PHL4}					44	
	t _{PLH4}					44	
Delay from A ₃ -A ₀ to F = 0	t _{PHL5}					48	
	t _{PLH5}					48	
Delay from A ₃ -A ₀ to OVR	t _{PHL6}					48	
	t _{PLH6}					48	
Delay from A ₃ -A ₀ to RAM ₃ and RAM ₀	t _{PHL7}					48	
	t _{PLH7}		48				
Delay from B ₃ -B ₀ to Y ₃ -Y ₀	t _{PHL8}		48				
	t _{PLH8}		48				
Delay from B ₃ -B ₀ to F ₃	t _{PHL9}		48				
	t _{PLH9}		48				
Delay from B ₃ -B ₀ to C _{n+4}	t _{PHL10}		48				
	t _{PLH10}		48				
Delay from B ₃ -B ₀ to G and P	t _{PHL11}		44				
	t _{PLH11}		44				
Delay from B ₃ -B ₀ to F = 0	t _{PHL12}		48				
	t _{PLH12}		48				
Delay from B ₃ -B ₀ to OVR	t _{PHL13}	C _L = 50 ±5 pF all outputs. See figure 5.		48			
	t _{PLH13}	R _L = 68 , R = 1.5k , Y ₃ -Y ₀ , G		48			

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 8

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit			
					Min	Max				
Delay from B ₃ -B ₀ to RAM ₃ and RAM ₀	t _{PHL14}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All		48	ns			
	t _{PLH14}					48				
Delay from D ₃ -D ₀ (ARITH) to Y ₃ -Y ₀	t _{PHL15}								37	
	t _{PLH15}								37	
Delay from D ₃ -D ₀ (ARITH) to F ₃	t _{PHL16}								37	
	t _{PLH16}								37	
Delay from D ₃ -D ₀ (ARITH) to C _{n+4}	t _{PHL17}								37	
	t _{PLH17}								37	
Delay from D ₃ -D ₀ (ARITH) to \bar{G} and \bar{P}	t _{PHL18}								34	
	t _{PLH18}								34	
Delay from D ₃ -D ₀ (ARITH) to F = 0	t _{PHL19}								40	
	t _{PLH19}								40	
Delay from D ₃ -D ₀ (ARITH) to OVR	t _{PHL20}								37	
	t _{PLH20}								37	
Delay from D ₃ -D ₀ (ARITH) to RAM ₃ and RAM ₀	t _{PHL21}								37	
	t _{PLH21}								37	
Delay from D ₃ -D ₀ (I = X37) to Y ₃ -Y ₀	t _{PHL22}								37	
	t _{PLH22}								37	
Delay from D ₃ -D ₀ (I = X37) to F ₃	t _{PHL23}								37	
	t _{PLH23}								37	
Delay from D ₃ -D ₀ (I = X37) to F = 0	t _{PHL24}				40					
	t _{PLH24}				40					
Delay from D ₃ -D ₀ (I = X37) to RAM ₃ and RAM ₀	t _{PHL25}				37					
	t _{PLH25}				37					
Delay from C _n to Y ₃ -Y ₀	t _{PHL26}				25					
	t _{PLH26}				25					
Delay from C _n to F ₃	t _{PHL27}				25					
	t _{PLH27}				25					
Delay from C _n to C _{n+4}	t _{PHL28}				21					
	t _{PLH28}				21					

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
Delay from C _n to F = 0	t _{PHL29}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All		28	ns	
	t _{PLH29}					28		
Delay from C _n to OVR	t _{PHL30}							25
	t _{PLH30}							25
Delay from C _n to RAM ₃ and RAM ₀	t _{PHL31}							28
	t _{PLH31}							28
Delay from I ₂ -I ₀ to Y ₃ -Y ₀	t _{PHL32}							40
	t _{PLH32}							40
Delay from I ₂ -I ₀ to F ₃	t _{PHL33}							40
	t _{PLH33}							40
Delay from I ₂ -I ₀ to C _{n+4}	t _{PHL34}							40
	t _{PLH34}							40
Delay from I ₂ -I ₀ to \overline{G} and \overline{P}	t _{PHL35}							44
	t _{PLH35}							44
Delay from I ₂ -I ₀ to F = 0	t _{PHL36}							44
	t _{PLH36}							44
Delay from I ₂ -I ₀ to OVR	t _{PHL37}							40
	t _{PLH37}							40
Delay from I ₂ -I ₀ to RAM ₃ and RAM ₀	t _{PHL38}							40
	t _{PLH38}							40
Delay from I ₅ -I ₃ to Y ₃ -Y ₀	t _{PHL39}			40				
	t _{PLH39}			40				
Delay from I ₅ -I ₃ to F ₃	t _{PHL40}			40				
	t _{PLH40}			40				
Delay from I ₅ -I ₃ to C _{n+4}	t _{PHL41}			40				
	t _{PLH41}			40				
Delay from I ₅ -I ₃ to \overline{G} and \overline{P}	t _{PHL42}			40				
	t _{PLH42}			40				
Delay from I ₅ -I ₃ to F = 0	t _{PHL43}			40				
	t _{PLH43}			40				

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 10

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay from I ₅ -I ₃ to OVR	t _{PHL44}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All		40	ns
	t _{PLH44}					40	
Delay from I ₅ -I ₃ to RAM ₃ and RAM ₀	t _{PHL45}					40	
	t _{PLH45}					40	
Delay from I ₈ -I ₆ to Y ₃ -Y ₀	t _{PHL46}					29	
	t _{PLH46}					29	
Delay from A ₃ -A ₀ (I = 2XX) to Y ₃ -Y ₀	t _{PHL47}					40	
	t _{PLH47}					40	
Delay from CP to Y ₃ -Y ₀	t _{PHL48}					40	
	t _{PLH48}					40	
Delay from CP to F ₃	t _{PHL49}					40	
	t _{PLH49}					40	
Delay from CP to C _{n+4}	t _{PHL50}					40	
	t _{PLH50}					40	
Delay from CP to \overline{G} and \overline{P}	t _{PHL51}					40	
	t _{PLH51}					40	
Delay from CP to F = 0	t _{PHL52}					40	
	t _{PLH52}					40	
Delay from CP to OVR	t _{PHL53}					40	
	t _{PLH53}					40	
Delay from CP to RAM ₃ and RAM ₀	t _{PHL54}					40	
	t _{PLH54}					40	
Delay from CP to Q ₃ and Q ₀	t _{PHL55}					33	
	t _{PLH55}					33	
Delay from \overline{OE} to Y ₃ -Y ₀	t _{PZL1}	C _L = 50 ±5 pF all outputs. See figure 5.				25	
	t _{PZH1}					25	
Delay from I ₈ to RAM ₃ and RAM ₀	t _{PZL2}					29	
	t _{PZH2}					29	
Delay from I ₈ to Q ₃ and Q ₀	t _{PZL3}					29	
	t _{PZH3}					29	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 11

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C T _c +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay from OE to Y ₃ -Y ₀ float <u>3/</u>	t _{PLZ1}	C _L = 50 ±5 pF all outputs. See figure 5.	9, 10, 11	All		25	ns
	t _{PHZ1}					25	
Delay from I _s to RAM ₃ and RAM ₀ float	t _{PLZ2}					29	
	t _{PHZ2}					29	
Delay from I _s to Q ₃ and Q ₀ float	t _{PLZ3}					29	
	t _{PHZ3}					29	
Minimum clock low time	t _{PWL}					15	
Minimum clock high time	t _{PWH}					15	
Minimum clock period	t _{cp}		32				

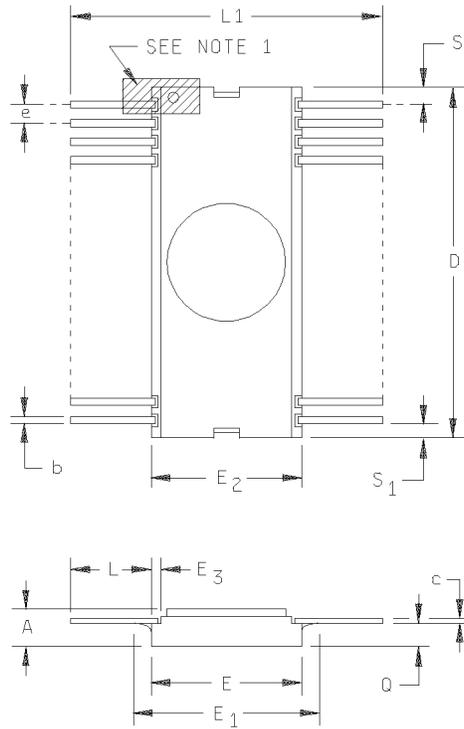
1/ These are three-state outputs internally connected to TTL inputs. The tri-state condition must be OFF.

2/ Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed 1 second.

3/ Output disable tests performed with C_L = 5 pF and measured to 0.5 V change of output voltage level.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 12

Case Outline Z



Dimensions									
Ltr.	Inches		Millimeters		Ltr.	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	.070	.098	1.78	2.49	E ₃	.030	---	0.76	---
b	.017	.023	0.43	0.58	e	.045	.055	1.14	1.40
c	.006	.010	0.15	0.25	L	.310	.370	7.87	9.40
D	1.050	1.090	26.67	27.69	L ₁	1.280	1.360	32.51	34.54
E	.620	.660	15.75	16.76	Q	.030	.060	0.76	1.52
E ₁	---	.680	---	17.27	S	---	.045	---	1.14
E ₂	.520	---	13.21	---	S ₁	.005	---	0.13	---

Notes:

1. Index area: A notch, tab, or pin one identificati on mark shall be located within the shaded area shown.
2. E₁ allows for Ag-Cu alloy brazed overrun.
3. Dimensions b and c increase by 3 mils maximum lim it is tinplate/solder dip lead finish is applied.
4. Dimensions are in inches.
5. Metric equivalents are given for general information only.

FIGURE 1. Case outlines .

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 13

Device type: 01			
Case outline Q			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A ₃	21	Q ₀
2	A ₂	22	D ₃
3	A ₁	23	D ₂
4	A ₀	24	D ₁
5	I ₆	25	D ₀
6	I ₈	26	I ₃
7	I ₇	27	I ₅
8	RAM ₃	28	I ₄
9	RAM ₀	29	C _n
10	V _{CC}	30	GND
11	F = 0	31	F ₃
12	I ₀	32	\overline{G}
13	I ₁	33	C _{n+4}
14	I ₂	34	OVR
15	CP	35	\overline{P}
16	Q ₃	36	Y ₀
17	B ₀	37	Y ₁
18	B ₁	38	Y ₂
19	B ₂	39	Y ₃
20	B ₃	40	\overline{OE}

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 14

Device types: 01			
Case outline Z			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I ₈	22	D ₀
2	I ₇	23	I ₃
3	RAM ₃	24	I ₅
4	NC	25	I ₄
5	RAM ₀	26	C _n
6	V _{CC}	27	GND
7	F = 0	28	F ₃
8	I ₀	29	\overline{G}
9	I ₁	30	C _{n+4}
10	I ₂	31	OVR
11	CP	32	\overline{P}
12	NC	33	Y ₀
13	Q ₃	34	Y ₁
14	B ₀	35	Y ₂
15	B ₁	36	Y ₃
16	B ₂	37	\overline{OE}
17	B ₃	38	A ₃
18	Q ₀	39	A ₂
19	D ₃	40	A ₁
20	D ₂	41	A ₀
21	D ₁	42	I ₆

NC =No connection

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 15

Micro code				ALU source operands	
I ₂	I ₁	I ₀	Octal code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

ALU Source Operand Control

Micro code				ALU function	Symbol
I ₅	I ₄	I ₃	Octal code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R S
H	L	L	4	R AND S	$\overline{R} S$
H	L	H	5	\overline{R} AND S	$\overline{R} S$
H	H	L	6	R EX-OR S	$R \overline{S}$
H	H	H	7	R EX-NOR S	$\overline{R \overline{S}}$

ALU Function Control

Micro code				RAM function		Q-REG function		Y Output	RAM shifter		Q shifter	
I ₈	I ₇	I ₆	Octal code	Shift	Load	Shift	Load		RAM ₀	RAM ₃	Q ₀	Q ₃
L	L	L	0	X	None	None	F Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F B	X	None	A	X	X	X	X
L	H	H	3	None	F B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 B	Down	Q/2 Q	F	F ₀	IN ₃	Q ₀	IN ₃
H	L	H	5	Down	F/2 B	X	None	F	F ₀	IN ₃	Q ₀	X
H	H	L	6	Up	2F B	Up	2Q Q	F	IN ₀	F ₃	IN ₀	Q ₃
H	H	H	7	Up	2F B	X	None	F	IN ₀	F ₃	X	Q ₃

X =Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the High-impedance state.

B =Register addressed by B inputs.

Up is toward MSS; Down is toward LSB.

ALU Destination Control

FIGURE 3. Truth tables and logic equations

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 16

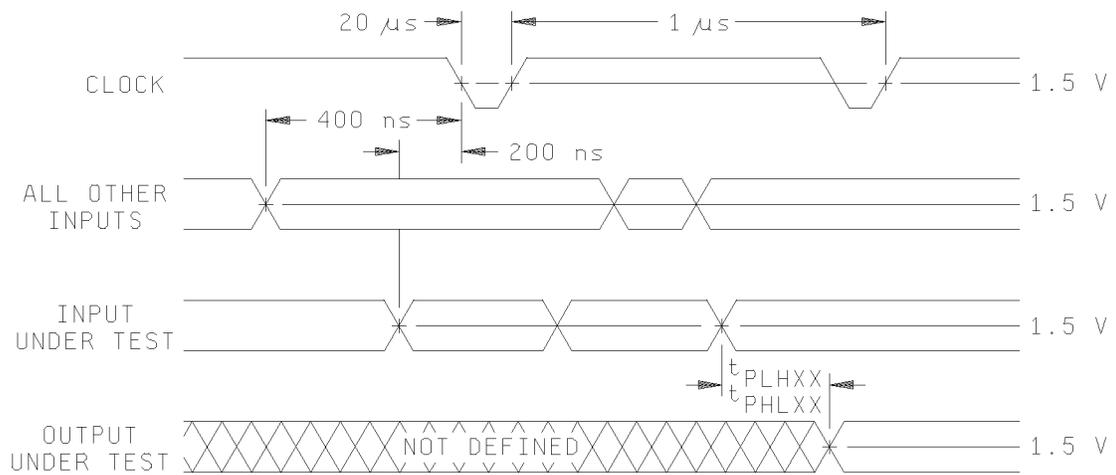
Octal I ₅₄₃ \ I ₂₁₀ Octal		0	1	2	3	4	5	6	7
		ALU Source A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C _n =L R Plus S C _n =H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1	C _n =L S Minus R C _n =H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
2	C _n =L R Minus S C _n =H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
3	R OR S	A Q	A B	Q	B	A	D A	D Q	D
4	R AND S	A Q	A B	0	0	0	D A	D Q	0
5	\overline{R} AND S	\overline{A} Q	\overline{A} B	Q	B	A	\overline{D} A	\overline{D} Q	0
6	R EX-OR S	$A \overline{Q}$	$A \overline{B}$	Q	B	A	$D \overline{A}$	$D \overline{Q}$	D
7	R EX-NOR S	$\overline{A \overline{Q}}$	$\overline{A \overline{B}}$	\overline{Q}	\overline{B}	\overline{A}	$\overline{D \overline{A}}$	$\overline{D \overline{Q}}$	\overline{D}

+=Plus
 -=Minus
 =OR
 =AND
 ^=EX-OR

Source Operand and ALU Function Matrix

FIGURE 3. Truth tables and logic equations - Continued.

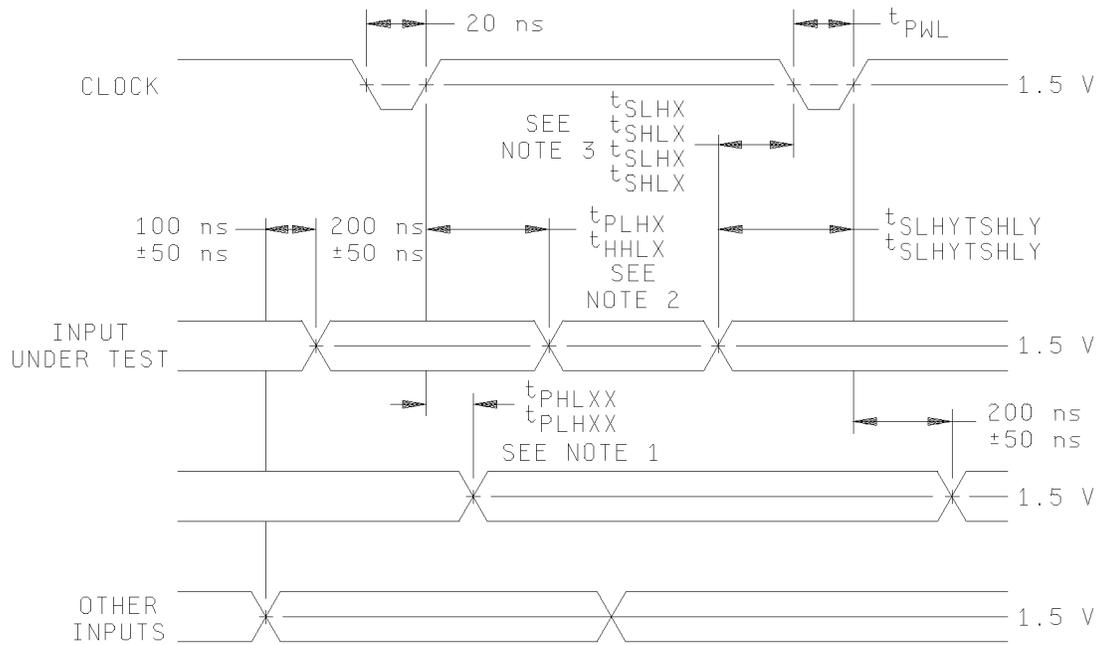
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 17



Note: For t_{PLHXX} , t_{PHLXX} , $XX = 01$ through 47 .

FIGURE 5. Switching waveforms and test circuits .

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 19



Notes:

1. For t_{PHLXX} and t_{PLHXX} , XX = 48 through 55. See table I for values.
2. For t_{HHLX} and t_{HLHX} , X = 1 through 7. See table I for values.
3. For $t_{SHLX \text{ or } Y}$ and $t_{SLHX \text{ or } Y}$, X = 2, 4, 5; Y = 1, 3, 6, 7, 8, 9, 10, 11, 12, and 13. See table I for values.

FIGURE 5. Switching waveforms and test circuits - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 20

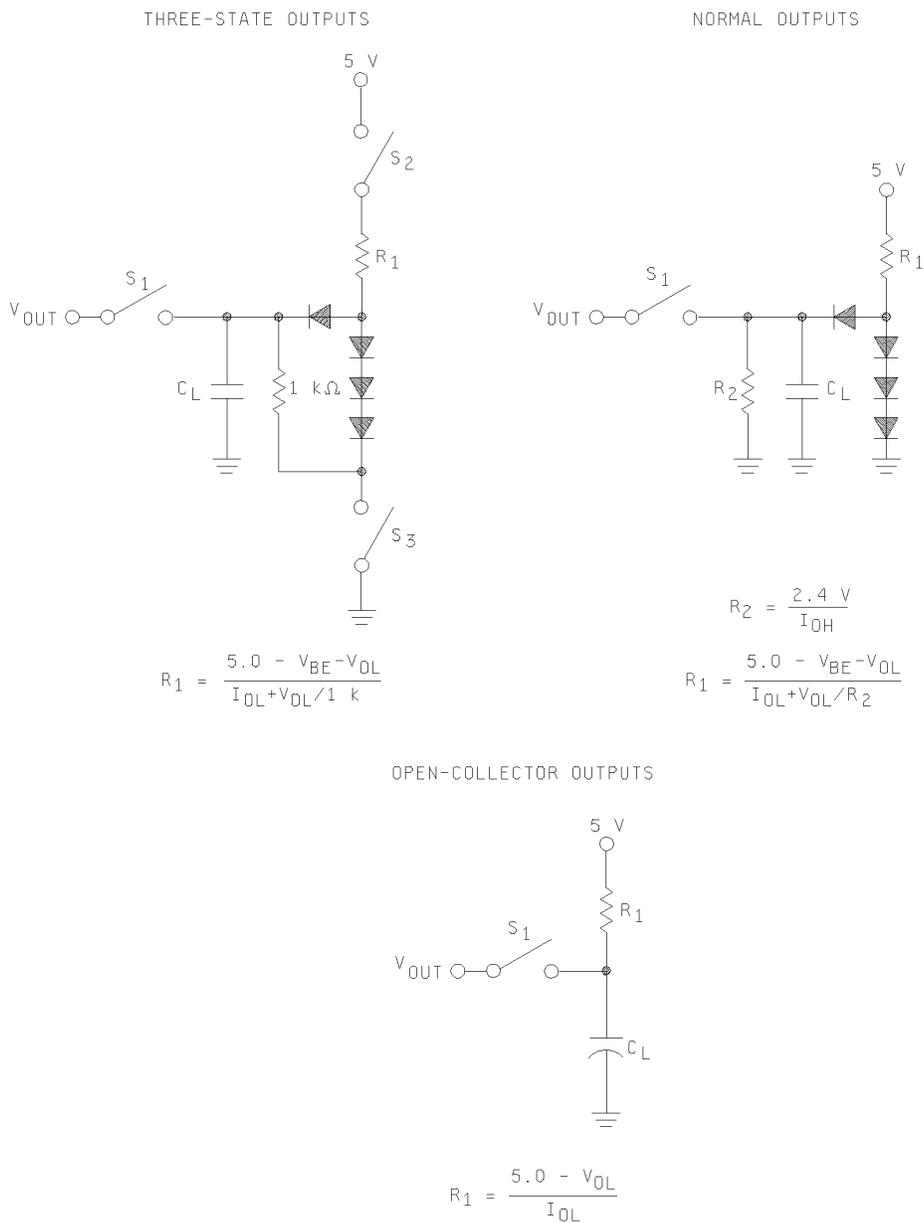


FIGURE 5. Switching waveforms and test circuits - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 21

Functional Pin	Test Circuit	R ₁	R ₂
RAM ₃	A	560	1 K
RAM ₀	A	560	1 K
F = 0	C	270	---
Q ₃	A	560	1 K
Q ₀	A	560	1 K
F ₃	B	620	3.9 K
G	B	220	1.5 K
C _{n+4}	B	360	2.4 K
OVR	B	470	3 K
P	B	470	3 K
Y ₀₋₃	A	220	1 K

Test Output Loads

Notes:

1. C_L = 50 pF, includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S₁, S₂, and S₃ are closed during function tests and all AC tests except output enable test.
3. S₁ and S₃ are closed while S₂ is open for t_{PZH} test.
S₁ and S₂ are closed while S₃ is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

FIGURE 5. Switching waveforms and test circuits - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 22

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the programming set and functionality of the device.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 23

4.3.2 Groups C and D inspections .

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125\text{ }^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements . The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use . Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability . Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's . All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users . Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments . Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply . Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		84057
		REVISION LEVEL D	SHEET 24

